



WAAS GUS Signal Generator

USER GUIDE

WAAS GUS Signal Generator User Guide

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Table of Contents

Customer Service	8
Notices	9
Foreword	10
1 Introduction	11
1.1 Features.....	13
1.2 Accessories and Options	13
1.3 Functional Overview	13
2 Minimum Connections	15
3 Setup Considerations	19
3.1 Front Panel Functionality	19
3.1.1 H/W Fault.....	19
3.1.2 10 MHz	19
3.1.3 CW Mode.....	19
3.1.4 Transmit Inhibit (Tx INHIBIT).....	19
3.1.5 Initiated Built in Test (IBIT)	20
3.1.6 1PPS	20
3.2 Rear Panel Functionality.....	20
3.2.1 Power	20
3.2.2 CW Switch	21
3.2.3 Ground Screw.....	21
3.2.4 CMP and WMP.....	21
3.2.5 Code PPS Output	21
3.2.6 1PPS In	21
3.2.7 10 MHz In and 10 MHz Out.....	21
3.2.8 RF Out.....	22
3.2.9 IF Out.....	22
4 Operation	24
4.1 Communications with the Signal Generator.....	24
4.1.1 Serial Port Default Settings	24
4.1.2 Communicating Using a Remote Terminal.....	24
4.1.3 Communicating Using a Personal Computer	24
4.2 Message Control and Data Lines.....	24
4.2.1 Other Control Lines	25
5 Messages	26
5.1 WMP Message Structure	26
5.1.1 Packet Synchronization Field	26
5.1.2 L1/L5 Indication Field	26
5.1.3 Command Message	27
5.1.4 Status Message.....	37
5.1.5 CRC-16/CCITT Checksum Field	44
5.2 Error Handling.....	44
6 Firmware Updates	46
6.1 Contacting the NovAtel Customer Support.....	46
6.2 Downloading the Files.....	47

6.3 Decompressing the Files	47
6.4 Running WinLoad	47
6.4.1 Open a File to Download	48
6.4.2 Downloading firmware	50
A Technical Specifications	51

Figures

1	WAAS GUS Signal Generator System Overview	12
2	Signal Generator	13
3	Interface Block Diagram	14
4	Signal Generator Setup Example	16
5	Coaxial Cable	17
6	Power Switch	17
7	Signal Generator Front Panel	19
8	Close-up of Connectors on Rear Panel	20
9	RS-485 Symbol Timing Diagram	25
10	Application of Frequency/Chipping Rate Ramp	35
11	Input Command Flowchart	36
12	Serial Number and Version Label	46
13	Main Screen of WinLoad	48
14	WinLoad's Open Dialog	48
15	Open File in WinLoad	49
16	COM Port Setup	49
17	Update Process Complete	50
18	Signal Generator Dimensions	51
19	Power Cable	55

Tables

1	External Reference Characteristics	21
2	L1 IF Bandwidth Requirements	22
3	IF Output Phase Noise	23
4	L5 IF Bandwidth Requirements	23
5	Packet Format	26
6	Packet Synchronization Field	26
7	Packet Synchronization Field Bit Format.....	26
8	L1/L5 Indication Field	27
9	L1/L5 Indication Bit Field	27
10	Command Message Fields.....	27
11	Command Message Identifier Field.....	28
12	Command Message Identifier Bit Fields.....	28
13	L1/L5 Control Command Bit Fields.....	28
14	L1/L5 Control Command Field.....	29
15	Resulting I Modulation Format.....	29
16	Resulting Q Modulation Format.....	30
17	L1 Initialization Command Fields	30
18	L5 Initialization Command Fields 500 SPS	31
19	Symbol Rate/RF Configuration Field	31
20	Sub-Chip Field.....	32
21	Code Chip Advance Field.....	32
22	Symbol Advance Field.....	32
23	L1 I Channel G2 Coder Initialization Field	32
24	L1 Q Channel G2 Coder Initialization Field	33
25	L5 I Channel XB(I) Coder Initialization Field.....	33
26	L5 Q Channel XB(Q) Coder Initialization Field	33
27	L1/L5 Code Chip Rate and Carrier Frequency Command Fields.....	34
28	Code Chip Rate Field	34
29	Code Chip Rate Ramp Field.....	34
30	Carrier Frequency Field Bit Format	34
31	Carrier Frequency Ramp Field Bit Format.....	35
32	Status Message Fields	37
33	Uplink Range Fields	37
34	Uplink Range Code Chip Sub-Phase Field	38
35	Uplink Range Code Chip Counter Field	38
36	Uplink Range Symbol Counter Field	38
37	Switch Status Field	38
38	Switch Status Bit Fields	38
39	Error Status Field.....	39
40	Error Status Bit Fields.....	39
41	Hardware Status Field	41
42	Hardware Status Bit Fields	41
43	Reset Command Second Epoch Counter	42
44	Hardware Reset Second Epoch Counter	42
45	Firmware Version Number Field.....	43
46	FPGA Version Number Field	43
47	Signal Generator State Field	43
48	Signal Generator State Value.....	43

49	CRC-16/CCITT Checksum Field.....	44
50	CRC-16/CCITT Checksum Field.....	44
51	CRC-16-CCITT Characteristics.....	44
52	Errors	45
53	Target Card Identification.....	49
54	L1 and L5 WMP Connector Pin-Out Descriptions	54
55	L1 and L5 CMP Connector Pin-Out Descriptions	54

Contact Information

If you have any questions or concerns regarding your WAAS GUS Signal Generator, please log a support request with NovAtel Customer Support using one of the following methods:

Log a Case and Search Knowledge:

Website: www.novatel.com/support

Log a Case, Search Knowledge and View Your Case History: (login access required)

Web Portal: <https://novatelsupport.force.com/community/login>

E-mail:

support@novatel.com

Telephone:

U.S. and Canada: 1-800-NOVATEL (1-800-668-2835)

International: +1-403-295-4900:

WAAS GUS Signal Generator Firmware Updates

Firmware updates are firmware revisions to an existing model, which improves basic functionality of the signal generator.

The process for obtaining firmware updates is discussed in *Chapter 6, Firmware Updates* starting on page 46. If you need further information, please contact NovAtel using one of the methods given above.

Notices

This equipment has been tested and found to comply with the limits for a class A digital device, pursuant to Part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment.

This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

Changes or modifications to this equipment not expressly approved by NovAtel Inc. could result in violation of FCC and CE Marking rules and void the user's authority to operate this equipment.

 To maintain compliance with the limits of a Class A digital device, you must use properly shielded interface cables when using the serial ports. Appropriate cables include Belden #9539, or equivalent, and Belden #8770 cable for input power source (ensuring the shield is connected to the protection ground).

 **CAUTION:**
Double pole/neutral fusing

 **CAUTION:**
The WAAS GUS Signal Generator must be installed in a Restricted Access Location only.

 Except for the externally accessible AC Fuses located on the rear panel, the WAAS GUS Signal Generator is not user-serviceable. In the event of any failure of the unit, do NOT remove any cards or covering panels from the unit. Return the unit to the factory for repair.

Where applicable, follow the electrical codes for the country of installation. Examples of country codes include:

- USA National Electrical Code (NFPA 70)
- Canada Canadian Electrical Code (CSA C22)
- UK British Standards Institute (BSI 7671)

Foreword

Congratulations!

Congratulations on your purchase of the Wide Area Augmentation System (WAAS) Signal Generator designed to generate a Ground Uplink Station (GUS) signal.

NovAtel is an industry leader in state-of-the-art GPS receiver and Signal Generator design. We believe that our WAAS GUS Signal Generator will meet your high expectations, and are working hard to ensure that future products and enhancements will maintain that level of satisfaction.

This is your primary hardware and software reference.

Scope

This manual contains sufficient information on the installation and operation of the WAAS GUS Signal Generator and its software to allow you to effectively integrate and fully operate it. It is beyond the scope of this manual to provide details on service or repair. Contact your local NovAtel dealer for any customer-service related inquiries.

The WAAS GUS Signal Generator utilizes a comprehensive user-interface command structure, which requires communications through its WAAS Message Processor (WMP) communications (COM) ports. WAAS GUS Signal Generator commands and logs can be found in *Chapter 5, Messages* starting on *Page 26*.

What's New in Rev 1 of this manual?

- Describes the WAAS GUS Signal Generator
- Quadrature channel enhancements
- Default and user selectable alternate RF output frequencies at a higher output signal level
- TNC or Type-N connectors used for RF external interfaces

Equipment Compatibility

The WAAS GUS Signal Generator (NovAtel P/N 01020347) is compatible with the legacy WAAS GUS-TYPE 1 Signal Generator (P/N 01017287) with the following exceptions and clarifications:

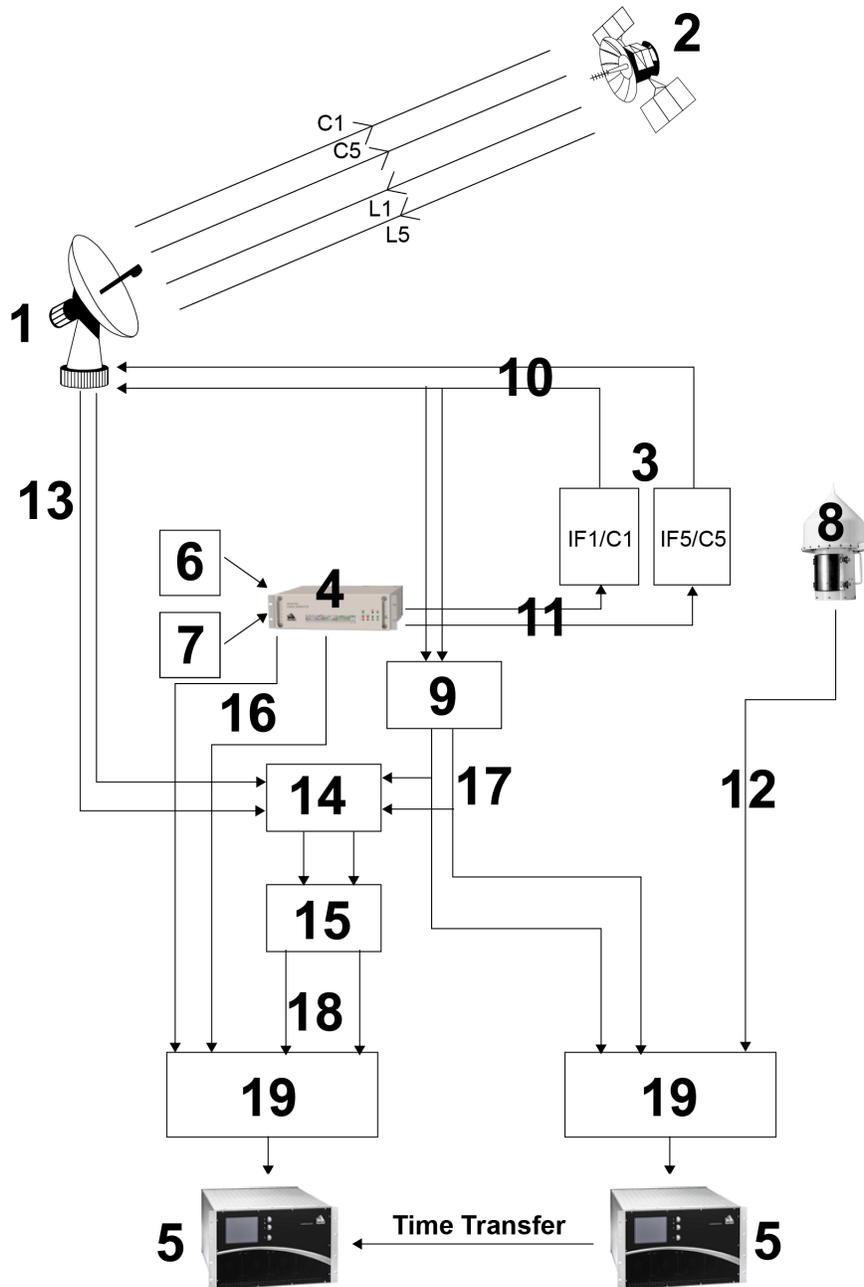
- The use of TNC connectors throughout (instead of BNC).
- The RF Output level has been increased to -50 dBm (from -100 dBm). The Main IF Output level of -20 dBm remains unchanged.
- Additional commands have been added to support additional functionality. The equipment will operate as the legacy unit when controlled with the legacy command set.

The WAAS GUS Signal Generator is a high performance L1/L5 Signal Generator. It generates a modulated Intermediate Frequency (IF) signal that is upconverted, amplified and transmitted to a Geo-stationary Earth Orbit (GEO) satellite. The primary GUS interfaces to the Signal Generator are the Safety Computer (SC), Radio Frequency Uplink (RFU) and Frequency Distribution Amplifier (FDA). The Signal Generator also provides, for L1:

- Coarse/Acquisition (C/A) codes with Pseudo Random Number (PRN) values of 120 to 158 inclusive (selectable via the initialization command)
- 70 MHz Binary-Phase Shift Keyed (BPSK) modulated or Quadrature-Phase Shift Keyed (QPSK) modulated IF output signal generation using the SBAS message with the selected 1023 bit PRN code
- In-phase (I) channel, I channel with dataless quadrature (Q) channel or I channel with independent data on the Q channel
- User configurable 1227.6 MHz (default) or 1575.42 MHz (alternate) RF output signal carrying the configured modulation for L1
- L5 codes with PRN values of 120 to 158 inclusive (selectable using the Initialization Command, see *Page 30*)
- 70 MHz BPSK or QPSK modulated IF output signal generation using the SBAS message with the selected 10230 bit PRN code
- In-phase Manchester encoded (I) channel, I channel with dataless quadrature (Q) channel or I channel with independent Manchester enclosed data on the Q channel
- User configurable 1176.45 MHz (default) or 1227.6 MHz (alternate) RF output signal carrying the configured modulation for L5

The Signal Generator consists of the Baseband Signal Generator (BSG), IF Signal Generator (ISG) and the Loopback Signal Generator (LSG). *Figure 1* shows an example of a system containing the Signal Generator and Receivers.

Figure 1: WAAS GUS Signal Generator System Overview



Reference	Description	Reference	Description
1	RFU antenna	11	L1/L5 IF signals
2	GEO satellite	12	L1 GPS, L2 GPS, L1 GEO, L5 GEO
3	RF Upconverter and Power Amplifier	13	L1/L5 RF loop back from satellite
4	WAAS GUS Signal Generator	14	RF Switch
5	Receiver (WAAS G-III)	15	L-Band Filter and Low Noise Amplifier
6	RS-485 message input from CMP	16	L1 and L5 at L2 SIGGEN RF loop
7	RS-232 command input from WMP	17	L1 and L5 TLT
8	GPS antenna	18	L1 and L5 GEO or TLT
9	Test loop translator	19	Power combiner/splitter
10	C1/C5 uplink		

Figure 1 shows a high level implementation of a WAAS GUS setup (see Chapter 2, Minimum Connections on Page 15 and Chapter 3, Setup Considerations on Page 19, for more information on this topic). Figure 2 shows the Signal Generator Front.

Figure 2: Signal Generator



1.1 Features

The Signal Generator has the following standard features:

- 19" rack-mountable 3U stainless steel enclosure
- NovAtel's advanced Signal Generator technology

1.2 Accessories and Options

The Signal Generator can be used with the following accessories:

- Power cable to connect the Signal Generator to a 100 to 240 V AC power source
- Optional Data Source Modules (used in a test environment and for firmware loading)
- Optional coaxial cables for the TNC and Type-N connectors on the Signal Generator
- Optional (WAAS G-III) Receiver

Should you need to order an accessory or a replacement part, contact NovAtel.

1.3 Functional Overview

The Signal Generator is comprised of two independent L1 and L5 generators which precisely control the frequency and phase of L1/L5 code and carrier signals and generate two independent L1 and L5 70 MHz IF signals. The L1 IF output has the L1 message structure with a factory configurable IF bandwidth of 2, 4 or 22 MHz for the Signal Generator. The L5 IF output has the L5 signal structure with an IF bandwidth of 22 MHz.

The Signal Generator provides two loopback signals that are monitored by the WAAS G-III Receiver. These RF signals are frequency upconverted replicas of the 70 MHz L1 and L5 outputs. By default, the 70 MHz L1 is upconverted to 1227.6 MHz. Similarly, by default, the 70 MHz L5 is upconverted to 1176.45 MHz. The user can select alternate RF frequencies of 1575.42 MHz for the L1 signal and 1227.6 MHz for the L5 signal.

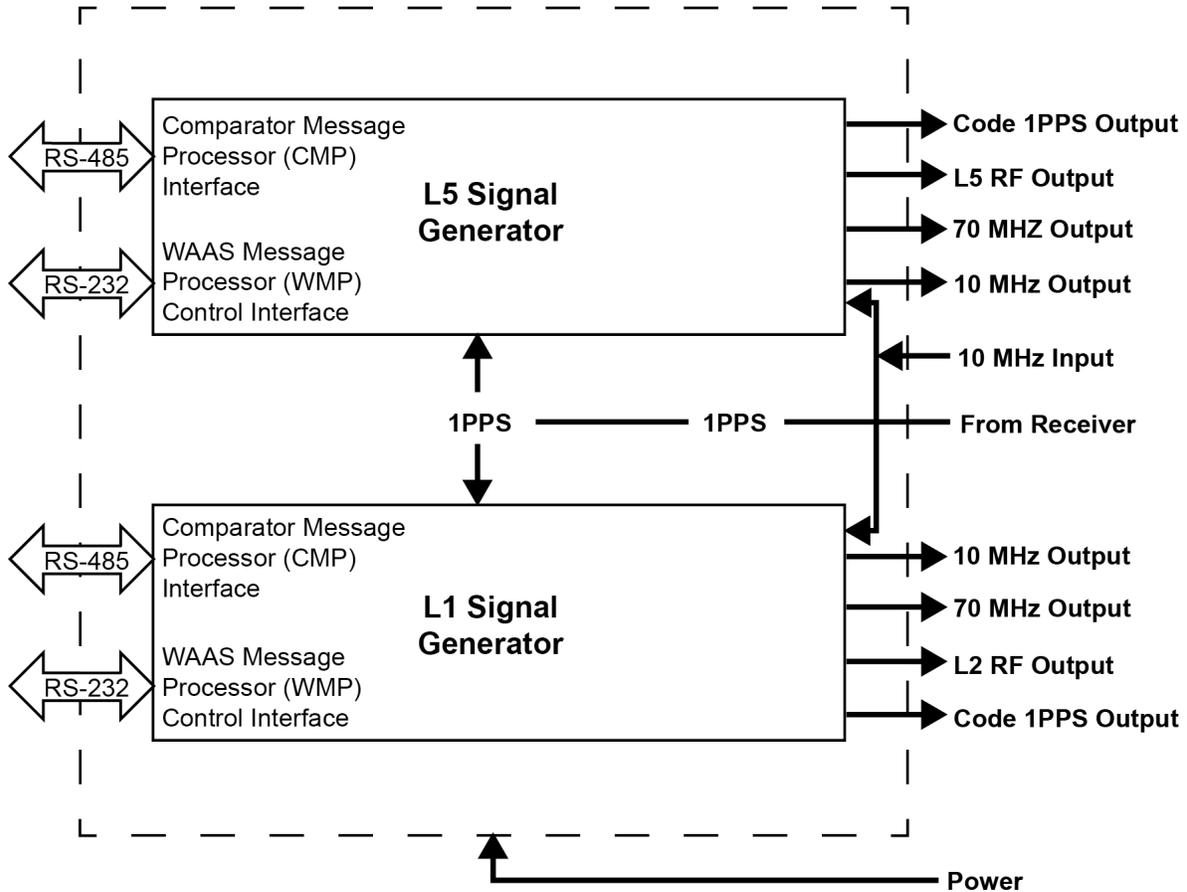
The L1 and L5 Signal Generators share a common 10 MHz frequency source from the GUS frequency standard and a 1PPS timing reference from the GUS receiver. The command and status interface between the Signal Generator and the WAAS GUS Message Processor (WMP) is independent for L1 and L5. Similarly, the message interface with the Comparator Message Processor (CMP) is independent for L1 and L5. This allows for independent L1 and L5 control and message data streams.

The primary signals generated are output on 70 MHz IF carriers which, outside the unit, are subsequently frequency upconverted to the necessary uplink frequencies. The Signal Generator contains facilities to precisely control the frequency and phase of both the code modulation and carrier of the generated signals.

A quadrature channel can be added to the L1 and L5 signals within the Signal Generator. When used, the normal signal is referred to as the I channel, and the quadrature signal is referred to as the Q channel. See also *Section 5.1.3.2, Control Command* starting on Page 28.

Figure 3 shows the interfaces of the Signal Generator.

Figure 3: Interface Block Diagram



After a cold start or after a power reset, the Signal Generator performs an Initiated Built-in Test (IBIT) memory self-test and internal calibration.

Provided a 1PPS reference source is made available to the Signal Generator, it can receive WAAS messages from the Safety Computer within 2 minutes of powering up.

When installed in a GUS, the Signal Generator requires the following connections:

AC Power - to the local mains supply to power the Signal Generator

L1 and/or L5 CMP - Comparator Message Processor as the WAAS message source

L1 and/or L5 WMP - WAAS Message Processor as the Signal Generator control terminal

10 MHz In - from the System 10 MHz Reference Source

1 PPS In - from the System 1 PPS Reference Source

L1 and/or L5 IF Output - to the Satellite Uplink path as the main Signal Generator output signal

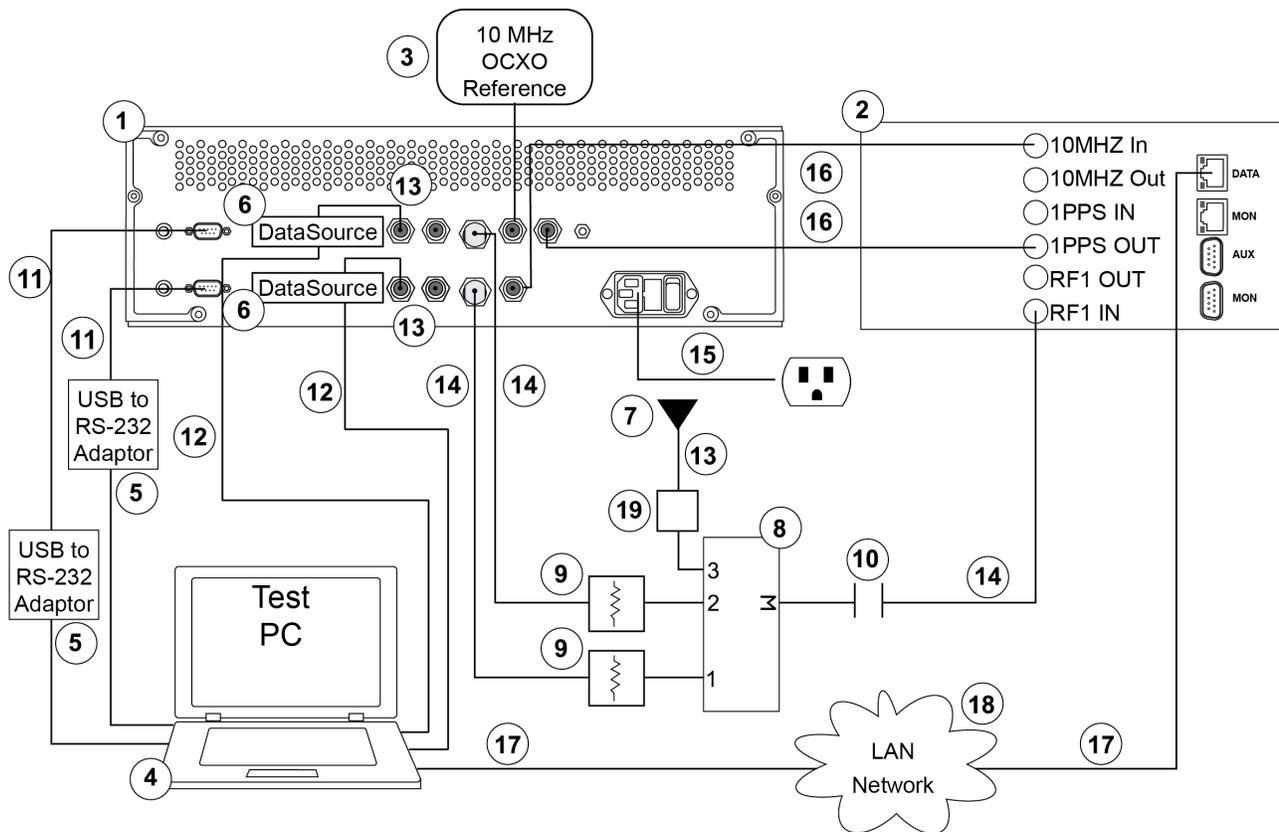
L1 and/or L5 RF Output - to the local Signal Generator signal monitoring facility

All of the above connections are described in more detail in Chapter 3, **Setup Considerations**.

To demonstrate and/or experiment with signals generated by the Signal Generator in a test environment, outside of the GUS, refer to the setup shown in *Figure 4* on *Page 16*. Additional information on using the Signal Generator in a test environment can be found in the WAAS SIGGEN GUI User Guide (NovAtel Document D25548) and WAAS SIGGEN UDSM User Guide (NovAtel Document D25598).

Figure 4 displays how you might typically set up the Signal Generator to test the signal.

Figure 4: Signal Generator Setup Example



Reference	Description
1	WAAS GUS Signal Generator (NovAtel P/N 1020347)
2	WAAS G-III Receiver (NovAtel P/N 01018740)
3	10 MHz Low Noise OCXO Reference Oscillator
4	Personal Computer (PC)
5	Off-the-Shelf USB to RS-232 Adapter
6	Data Source Module (NovAtel P/N 01020346)
7	Externally Powered GPS Antenna
8	50 Ohm 3:1 RF Combiner, SMA
9	50 dB SMA Coaxial Attenuators, 50 ohm
10	SMA Coaxial DC-block (the WAAS G-III Receiver RF1 In outputs DC power by default)
11	DB-9 Serial Cable
12	USB Cable Type-A to micro-USB (NovAtel P/N 60723119)
13	50 ohm Coaxial Cable, Male TNC to Male SMA (NovAtel P/N 60423064)
14	50 ohm Coaxial Cable, Male Type-N TNC to Male SMA
15	120 VAC Power Cable (NovAtel P/N 60723070)
16	50 ohm Coaxial Cable, Male TNC to Male TNC
17	CAT-5 Ethernet Cable
18	Local Area Network
19	Gain Element (either an amplifier or an attenuator) ¹

1. To guarantee the noise power is between -152 dBm/Hz and -132 dBm/Hz at the input to the receiver. The normal tracking range of the receiver is for CNos between 30 dB/Hz and 60 dB/Hz.

An example configuration would result from the following steps (see also *Figure 4*):

1. Place the Signal Generator on a suitable work surface.
2. Connect the 1PPS In port on the Signal Generator to the 1PPS Out port on the Receiver with interconnecting coaxial cable. A typical coaxial cable is shown in *Figure 5*.

Figure 5: Coaxial Cable



3. Connect the 10 MHz In port on the Signal Generator to the 10 MHz external reference with an interconnecting coaxial cable.
4. Connect the 10 MHz In port on the Receiver to the 10 MHz Out port on the Signal Generator with an interconnecting coaxial cable.
5. Connect the L1 and L5 CMP ports and the L1 and L5 Code 1PPS Out ports on the Signal Generator to their respective Data Source Modules. Set the Data Source Modules L1 and L5 selector switches respectively.
6. Connect the Data Source Modules to the Test PC using the USB cables supplied with the Data Source.
7. Connect the L1 and L5 RF OUT ports on the Signal Generator to attenuators which are then connected to inputs of the RF Combiner using interconnecting coaxial cables. The attenuators should be selected so that the signal power at the receiver input is between -105 to -90 dBm given an input noise power density to the receiver of -150 dBm/Hz. (Typical attenuator values are approximately 50dB.)
8. Connect a Powered GPS Antenna to a LNA which is then connected to the input of the RF Combiner using interconnecting coaxial cables. The total gain due to the antenna LNA, cable losses, combiner and any external LNA should be approximately +20 dB or equivalently the noise power provided at the receiver input, accounting for cascaded gain and noise figure, should be approximately -150 dBm/Hz.
9. Connect the output of the RF Combiner to a DC Block which is then connected to the RF1 In of the Receiver using interconnecting coaxial cables.
10. Connect the L1 and L5 WMP ports on the Signal Generator to a serial port on your PC with serial data cables.
11. Connect the Data port on the Receiver to the same LAN that your Test PC is connected to using a network cable.
12. Connect AC power to the power input port on the back of the Signal Generator using the supplied power cable. Similarly, power the receiver and ensure your PCs are powered.
13. Press the power switch on the back of the Signal Generator, see *Figure 6*. The Power LED on the front panel glows green while power is applied.

Figure 6: Power Switch



14. Control the Signal Generator using the Signal Generator GUI running on the Test PC.

15. Monitor your L1 and L5 data using available logs and commands from the Receiver through the Test PC.

The sections of *Chapter 3, Setup Considerations on Page 19* give further details on steps #1 to #13 while *Chapter 4, Operation on Page 24* helps with step #14. See the Signal Generator specific command and logs in *Chapter 5, Messages on Page 26*. For other commands and logs available with the Receiver, please refer to its WAAS G-III Reference Receiver user manual (*OM-20000137*).

The Signal Generator is a device that is intended for use in dry stable environments.



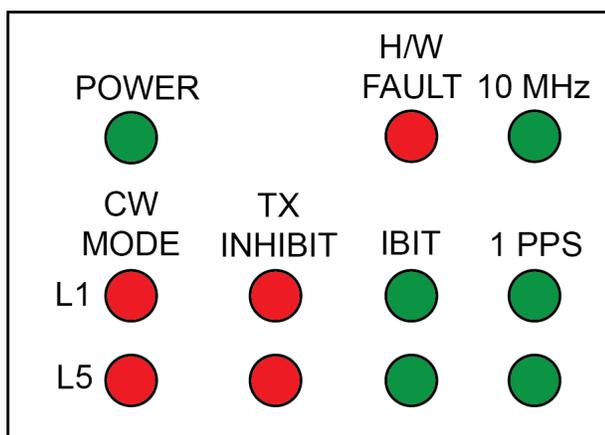
Observe ventilation requirements.

For proper ventilation, the Signal Generator requires clearance of 6 inches minimum on all sides, except for the rear panel, which should remain clear from obstructions. Installations not meeting this requirement must ensure a minimum forced air flow rate of 1 cu-m/minute through the ventilation holes of the unit.

3.1 Front Panel Functionality

As seen in *Figure 7*, there is a power LED that glows green when power is applied to the Signal Generator.

Figure 7: Signal Generator Front Panel



3.1.1 H/W Fault

This LED glows red when there is an internal hardware fault. It will cycle on and off at a 1 Hz rate when the 1PPS input signal is lost. See also *Section 5.1.4.6, Hardware Status Fields on Page 41*.

3.1.2 10 MHz

This LED glows green when there is a 10 MHz reference present. The 10 MHz reference input level is in the range +12 to +14 dBm and has an impedance of 50 ohms.

3.1.3 CW Mode

When the L1 CW Only or L5 CW Only switch is manually selected, the Signal Generator removes all modulation from the L1 or L5 signal carrier respectively. The corresponding LED on the front panel glows red at the same time.

3.1.4 Transmit Inhibit (Tx INHIBIT)

This L1 or L5 Tx INHIBIT LED glows red if the L1 or L5 IF output is disabled. Incomplete L1 or L5 message data transfer forces the unit to inhibit L1 or L5 signal transmission respectively for one second following the error.

This transmit inhibit function is controlled by a discrete signal that is applied via the Comparator input port. This function is fail safe, so that if the control lines become open the transmission is inhibited.

3.1.5 Initiated Built in Test (IBIT)

IBIT is performed at power-up or upon a hardware reset. IBIT includes ROM and RAM testing. The front panel specifies whether the L1 or L5 IBIT passed or failed. A green LED signifies an IBIT pass and an unlit LED signifies an IBIT failure.

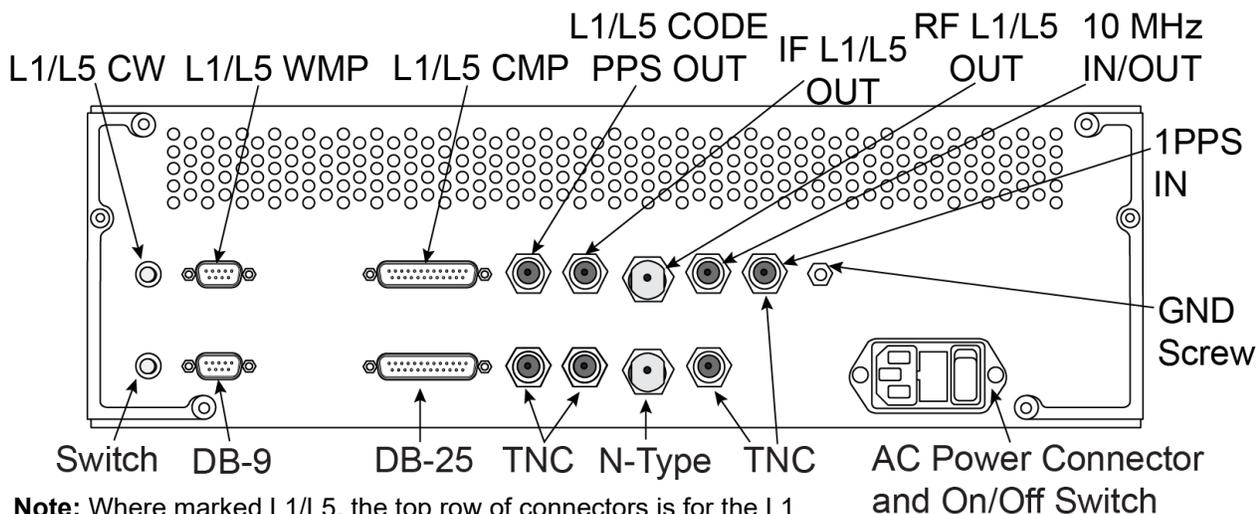
3.1.6 1PPS

The 1PPS LEDs are green and will cycle on and off at a 1 Hz rate to indicate the presence of a 1PPS output signal.

3.2 Rear Panel Functionality

The connections on the rear panel and their connector types are shown in *Figure 8*.

Figure 8: Close-up of Connectors on Rear Panel



Note: Where marked L1/L5, the top row of connectors is for the L1 signal and bottom row of connectors is for the L5 signal. Likewise for the 10 MHz In/Out, the top connector is the Input and the bottom is the Output.

Each connector is keyed to ensure that the cable can be inserted in only one way, to prevent damage to both the Signal Generator and the cables. Furthermore, the connectors that are used to mate the cables to the Signal Generator require careful insertion and removal. Observe the following when handling the cables.

- To insert a cable, make certain you are using the appropriate cable for the port - the serial cable has a different connector (DB9) than the PPS cable (TNC), or the RF cable (N-Type) connectors.



DO NOT PULL DIRECTLY ON THE CABLES.

3.2.1 Power

After initial connection of the power supply to the Signal Generator and pressing the power switch on the back of the unit (see Figure 8 above), the Power LED on the front of the unit (see Figure 7 on Page 19) glows green.

The Signal Generator requires an input supply voltage that comes from a normal power source of 120 volts AC at 60 Hz or 230 volts AC at 50 Hz through its 3-pin (hot, neutral and ground) power connector.



For safety reasons, ensure the 3-pin AC power plug is connected to a properly grounded AC mains supply.

The AC Power Connector on the Signal Generator contains two 5 x 20 mm, 2.5 A slow-blow fuses that can be serviced as long as the Signal Generator is disconnected from power. Fuses are accessed by pressing the upper and lower tabs of the integrated fuse holder located between the AC Power connector and ON/OFF Switch. Use only Littelfuse ® P/N 021802.5MXP or equivalent.



Blown fuses usually indicate that the internal hardware is malfunctioning. The hardware should be returned to the factory for diagnosis and repair.

For a listing of the required input supply voltages, see *Input/Output Connectors on Page 52*. For more information on the supplied 3-pin power cable, see *Section A.1.2.1, Power Cable on Page 55*.

3.2.2 CW Switch

The Signal Generator provides a L1 CW and a L5 CW toggle switch with a mechanical latching mechanism which remove all modulation from the L1 IF and RF or L5 IF and RF carriers respectively.

3.2.3 Ground Screw

The available length of the stud is 3/8". The stud is an 8-32 thread.

3.2.4 CMP and WMP

Each Signal Generator has independent command and status interfaces, and communicates over this interface with a host computer (WAAS Message Processor - WMP). Similarly, the message interface for each Signal Generator is independent, and communicates with a message generator (the Comparator Message Processor - CMP).

The Signal Generator is capable of L1 or L5 communications via two ports, L1 WMP and L5 WMP respectively.

3.2.5 Code PPS Output

The L1 and L5 Code PPS Out ports allow synchronization of external test equipment with the modulated L1 or L5 signal available respectively.

3.2.6 1PPS In

The 1PPS level is an active low pulse with TTL levels driving an input impedance of 3 k Ω . It is also factory configurable to use active high pulses and/or a 50 Ω AC coupled input impedance.

The pulse width of the 1PPS update is 200 microseconds nominally with a repetition rate of 1PPS. The high to low transition is the reference edge. The high to low transition time is 5 ns or less. The high to low transition jitter with respect to the 10 MHz is 1 ns or less.

Use of an external 50 ohm feed-thru terminator is recommended for factory default configuration.

For further information on the electrical specifications or connector type for the 1PPS In port, please see *Input/Output Connectors on Page 52*.

3.2.7 10 MHz In and 10 MHz Out

There are two reference signal TNC connectors on the back of the Signal Generator for 10 MHz In and 10 MHz Out.

The Signal Generator contains a detection mechanism and will use a 10 MHz reference signal when provided. In the absence of an external 10 MHz reference signal, the signal generator will use its own internal 10 MHz OCXO. Proper operation of the Signal Generator requires that the performance of the 10 MHz reference signal have the characteristics provided in *Table 1* below.

Table 1: External Reference Characteristics

Frequency	10 MHz
Amplitude	13 dBm \pm 1 dBm

Impedance	50 ohms	
Phase Noise	Offset from Carrier	Phase Noise
	1 Hz	<-100 dBc/Hz
	10 Hz	<-130 dBc/Hz
	100 Hz	<-145 dBc/Hz
	1000 Hz	<-150 dBc/Hz
	10,000 Hz	<-154 dBc/Hz
100,000Hz	<-154 dBc/Hz	
Accuracy	$\pm 5 \times 10^{-13}$	

The 10 MHz output is buffered from the current system reference signal which may be the Signal Generator's internal OCXO or an external 10 MHz input. Its output amplitude is in the range 0 to +6 dBm and its output impedance is 50 ohms.

For further information on the signals or connector type for the 10 MHz In and 10 MHz Out ports, please see *Input/Output Connectors* on Page 52.

3.2.8 RF Out

The L1 and L5 RF Out connectors provide Radio Frequency (RF) signals from the Signal Generator.

The Signal Generator contains RF circuits to modulate and convert the digital In-Phase and Quadrature (I and Q) data streams to an RF signal spectrum.

The nominal level of the RF Output of the Signal Generator is -50 dBm. The default frequency of the L1 RF Output is 1227.6 MHz and can be user configured for an alternate output frequency of 1575.42 MHz. The default frequency of the L5 RF Output is 1176.45 MHz and can be user configured for an alternate output frequency of 1227.6 MHz.

The Signal Generator L1 RF output is BPSK or QPSK modulated at a 1.023 MHz chip rate. The L5 RF output modulation chip rate is 10.23 MHz. The RF output modulator phase on accuracy is within ± 3 degrees.

For further information on the signals or connector type for the RF Out connectors, please see *Input/Output Connectors* on Page 52.

3.2.9 IF Out

The L1 and L5 IF Out connectors provide a 70 MHz Intermediate Frequency (IF) signals from the Signal Generator. It is normally used to provide L1 and L5 signals that are unconverted and uplinked to the GEO satellite at the appropriate C band frequencies.

The signal amplitude is within the range $-20 \text{ dBm} \pm 1.0 \text{ dB}$ for any specified I/Q configuration. The signal amplitude is stable to within 0.25 dB over an ambient operating temperature of 15°C to 25°C. After a warmup period of 1 hour, the L1 IF signal amplitude is stable to within 0.25 dB over a 24 hour period at a constant ambient temperature.

The factory configurable L1 signal (2, 4 or 22 MHz) is filtered by IF filters having the characteristics described in Table 2.

Table 2: L1 IF Bandwidth Requirements

Nominal Bandwidth	3 dB Bandwidth	40 dB Bandwidth
2 MHz	$\geq 1.9 \text{ MHz}$	$\leq 4.25 \text{ MHz}$
4 MHz	$\geq 4 \text{ MHz}$	$\leq 11.2 \text{ MHz}$
22 MHz	$\geq 22 \text{ MHz}$	$\leq 28 \text{ MHz}$

The IF output has the phase noise characteristic shown in *Table 3*.

Table 3: IF Output Phase Noise

Offset from Carrier	Phase Noise (\leq)
1 Hz	-65 dBc/Hz
10 Hz	-85 dBc/Hz
100 Hz	-90 dBc/Hz
1 KHz	-95 dBc/Hz
10 KHz	-100 dBc/Hz
100 KHz	-108 dBc/Hz

The L1 CW Only switch forces the unit to remove all modulation from the signal carrier (I and Q signals both forced to zero).

Disabling of the L1 output signal from the Signal Generator occurs under specific operating conditions identified in *Section 5.2, Error Handling on Page 44*.

The L5 signal is filtered with a 22 MHz IF filter having the characteristics described in *Table 4*.

Table 4: L5 IF Bandwidth Requirements

Nominal Bandwidth	3 dB Bandwidth	40 dB Bandwidth
22 MHz	≥ 22 MHz	≤ 28 MHz

The L5 CW Only switch forces the unit to remove all modulation from the signal carrier (I and Q signals both forced to zero).

The output impedance for the L1 and L5 IF Output is 50 Ohms.

Before operating the Signal Generator for the first time, ensure that you have followed the installation instructions of *Chapter 2, Minimum Connections on Page 15* and *Chapter 3, Setup Considerations on Page 19*. The following instructions are based on a configuration such as that shown in “*Signal Generator Setup Example*” on page 16. It is assumed that a personal computer is used during the initial operation and testing for greater ease and versatility.

4.1 Communications with the Signal Generator

Communication with the Signal Generator is straightforward, and consists of issuing commands through the WMP communication ports from an external serial communications device. This could be either a terminal or a PC that is directly connected to the Signal Generator serial port using an extension cable. For information about commands and logs that are useful for basic operation of the Signal Generator, please see *Chapter 5, Messages on Page 26*.

4.1.1 Serial Port Default Settings

The Signal Generator communicates with your PC or terminal via the communication ports. For communication to occur, both the Signal Generator and the operator interface have to be configured properly. The Signal Generator data ports’ settings are as follows:

- 19200 bps, odd parity, 8 data bits, 1 stop bit, cts/rts handshaking, echo off

4.1.2 Communicating Using a Remote Terminal

One method of communicating with the Signal Generator is through a remote terminal. The Signal Generator allows proper RS232 interface with your data terminal. To communicate with the terminal, the Signal Generator requires the RX, TX, RTS, CTS and GND lines to be used. Ensure that the terminal’s communications set-up matches the Signal Generator’s RS232 protocol.

4.1.3 Communicating Using a Personal Computer

A PC can be set up to emulate a remote terminal as well as provide the added flexibility of creating multiple-command batch files and data logging storage files. Any standard communications software package that emulates a terminal can be used to establish bidirectional communications with the Signal Generator. No particular terminal type is assured. All data is sent as raw characters.

You can create command batch files using any text editor; these can then be directed to the data port that is connected to the Signal Generator using a communications software package. This is discussed later in this chapter.

4.2 Message Control and Data Lines

The signal generator will modulate CMP messages onto the carrier if a complete CMP message is received in the period between 20 ms and 980 ms after the respective L1 1 PPS or L5 1 PPS pulse.



Nominal GUS operation can use the reference 1 PPS to trigger the transmission of a CMP message as the L1 1 PPS and L5 1 PPS pulses should be in advance of the external 1 PPS by about 130 ms.

The Message Interface provides the necessary control and data lines to allow downloading of data symbols from the CMP to the Signal Generator. These lines are:

- MSGRDY from CMP to Signal Generator
- MSGCLK from Signal Generator to CMP
- MSGDATA from CMP to Signal Generator

After a compared message is stored in the Comparator output buffer, the Comparator sets the Message Ready flag to the Signal Generator.

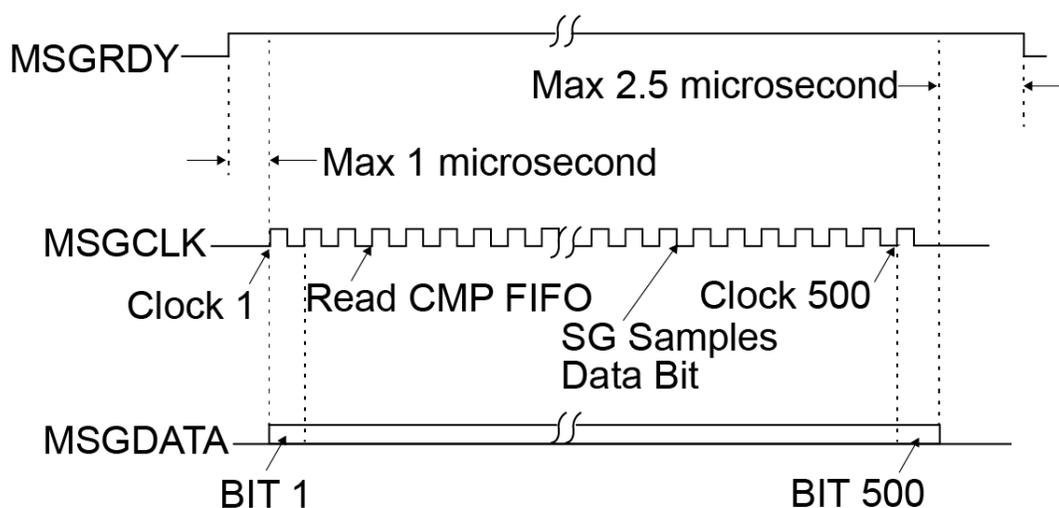
The Message Ready signal enables the Signal Generator internal 1 MHz clock (period 1 ms) which is then returned to the Comparator.

The Comparator counts 500 clocks and resets the Message Ready flag after the 500th clock. For each clock, the Comparator transfers each data bit from its output buffer on the leading edge, and the Signal Generator samples the data bit on the trailing edge. The 500 bits of data are then transferred from the CMP to the Signal Generator at the 1 MHz rate. The entire transfer takes 500 μ s or 1/2 ms. The Signal Generator buffers each L1 and L5 500 SPS message from the CMP.

If quadrature (Q) data is enabled on the L1 or L5 interface, a second set of 500 bits must be provided by the Comparator for that interface as the Q data. If the second set of 500 bits is not provided, no data shall be transmitted and the output of both the I and Q shall be inhibited. If only in-phase (I) data is enabled and a second set of 500 bits is provided, the second set of 500 bits shall be discarded, however, the first set of 500 bits shall be transmitted normally as the I data.

After MSGRDY has been asserted, the Signal Generator sends its first clock within 1 microsecond of the assertion. After the 500th clock goes low, the MSGRDY should not be reasserted until after another 4 microseconds. The interface timing is shown in *Figure 9*.

Figure 9: RS-485 Symbol Timing Diagram



4.2.1 Other Control Lines

Two other control lines exist on the Message Interface. These are:

- RESET from CMP to Signal Generator
- TX INH from CMP to Signal Generator

If the RESET line is high, the Signal Generator hardware undergoes a hard reset. The Signal Generator is rebooted to power-up state after the RESET line is de-asserted. Note, the L1 and L5 operations are independent.

If the TX INH line is high, the Signal Generator IF output switch opens, causing the IF output signal to cease. The RF output is not switched.

5.1 WMP Message Structure

Command and status messages are exchanged between the WMP and the Signal Generator using a RS-232 link. Both command and status messages are encapsulated in a fixed length packet. This packet contains a synchronization field, a L1/L5 indication field, message data fields and a CRC field for reliable packet transfer. *Table 5* shows the format of a message packet. Binary messages (command or status) are received by the Signal Generator in byte order [0] through [35]. The Signal Generator swaps these bytes as necessary in order to recover the original data fields. The tables shown in this chapter indicate the order in which bytes are received and transmitted by the Signal Generator.

Table 5: Packet Format

Field	Bytes	Byte Position	Description
1	4	Byte [0:3]	Packet Synchronization Bytes Field (start of packet)
2	1	Byte [4:4]	L1/L5 Indication Field
3	29	Byte [5:33]	Command Message Payload Fields or Status Message Payload Fields.
4	2	Byte [34:35]	16 bit CRC Field.

5.1.1 Packet Synchronization Field

The packet synchronization field consists of four (4) bytes containing the hex value 0xAA5555AA. The Signal Generator looks for these synchronization bytes and interprets them to be the start of a new packet. Status messages transmitted to the WMP also have these synchronization bytes encoded to the hex value 0xAA5555AA. *Table 6* shows the Packet Synchronization field. *Table 7* shows the Packet Synchronization field byte and bit order.

Table 6: Packet Synchronization Field

Field	Bytes	Byte Position	Description	Value
1	4	Byte [0:3]	Start of packet	0xAA5555AA

Table 7: Packet Synchronization Field Bit Format

Byte [0]	Byte [1]	Byte [2]	Byte [3]
D7 - D0	D15 - D8	D23 - D16	D31 - D25
D0 = LSB			D31 = MSB
0xAA	0x55	0x55	0xAA

5.1.2 L1/L5 Indication Field

This field consists of one (1) byte containing the L1 or L5 indication flag. If a command is targeted for a L1 Signal Generator then this byte contains the integer value 1, otherwise the integer value 5 is used to indicate a L5 target. If a L1 signal generates a status message, this byte contains the integer value 1, otherwise the integer value 5 is used to indicate a L5 signal generation source. *Table 8* shows the L1/L5 Indication field. *Table 9 on Page 27* shows the L1/L5 Indication field bit order.

Table 8: L1/L5 Indication Field

Field	Bytes	Byte Position	L1/L5 Destination	WMP Destination
2	1	Byte [4:4]	L1=1, L5=5	1=L1, L5=5

Table 9: L1/L5 Indication Bit Field

Byte [4]							
D7	D6	D5	D4	D3	D2	D1	D0
MSB							LSB

5.1.3 Command Message

Table 10 shows the command message fields. The sections that follow indicate the data fields for all valid command message identifiers.

Table 10: Command Message Fields

Field	Bytes	Byte Position	Description
3-1	1	Byte [5:5]	Command Message Identifier Field
3-2	1	Byte [6:6]	Control Command Data Field
3-3	1	Byte [7:7]	Symbol Rate Field
3-4	1	Byte [8:8]	Sub-Chip Field
3-5	2	Byte [9:10]	Code Chip Advance Field
3-6	2	Byte [11:12]	Symbol Advance Field
3-7	2	Byte [13:14]	L1 I coder init G2 Field or L5 I coder init XB(I) Field
3-8	2	Byte [15:16]	L1 Q coder init G2 Field or L5 Q coder init XB(Q) Field
3-9	6	Byte [17:22]	Code Chip Rate Field
3-10	2	Byte [23:24]	Code Chip Rate Ramp Field
3-11	6	Byte [25:30]	Carrier Frequency Field
3-12	3	Byte [31:33]	Carrier Frequency Ramp Field

5.1.3.1 Command Message Identifier Field

The Command Message Identifier field consists of one byte containing the command (instruction) message ID. Based on this ID, the Signal Generator knows which data fields to interpret and what command needs to be executed. Table 11 shows the Command Message Identifier byte field and bit order. Table 12 on Page 28 shows the Command Message Identifier bit fields.

Table 11: Command Message Identifier Field

Byte [5]							
D7	D6	D5	D4	D3	D2	D1	D0
MSB							LSB

Table 12: Command Message Identifier Bit Fields

Bit	Command message (WMP to Signal Generator)	Command Message ID Field
D0	Control Command	0x01
D1	Initialization Command	0x02
D2	Code Chip Rate and Carrier Frequency Command	0x04
D3	Reserved for future use	0x08
D4	Reset Command	0x10
D5	Reserved for future use	0x20
D6	Reserved for future use	0x40
D7	Reserved for future use	0x80

5.1.3.2 Control Command

The Control Command provides for synchronous initialization of the L1 I and Q C/A code Generator states or the L5 I and Q XB code Generator states, code modulation, symbol modulation, I channel modulation or Q channel modulation. Upon receiving this command, the coder commences execution at the occurrence of the next 1-PPS update pulse. If a valid Initialization Command was not received prior to receiving this command, this command is not executed and the status message indicates the error. The Control command packet contains one byte of data.

Table 13 on Page 28 shows the L1/L5 Control Command byte field and bit order. *Table 13* below shows the L1/L5 Control Command bit fields. This command must be preceded by an Initialization command to ensure that the I and Q coders have been reset, initialized and advanced to the correct state.

Table 13: L1/L5 Control Command Bit Fields

Bit	Description	Range	Purpose
D0	Initialize Range	0 - 1	1 = Start coders at next valid Reference 1PPS pulse
D1	Disable PRN Code (I)	0 - 1	1 = Coder output not used in modulation
D2	Disable Message (I)	0 - 1	1 = Symbol not used in modulation
D3	BPSK/QPSK Modulation Mode Select	0 - 1	0 = BPSK 1 = QPSK
D4	Disable NH/Manchester (Q)	0 - 1	1=Disable NH code for dataless operation and Manchester Code for data operation
D5	Disable NH/Manchester (I)	0 - 1	1=Disable NH code for dataless operation and Manchester Code on data for L5 (not used for L1 I data)
D6	Disable Message (Q)	0 - 1	1=Symbol not used in modulation
D7	Disable PRN Code (Q)	0 - 1	1=Coder output not used in modulation

Table 14: L1/L5 Control Command Field

Byte [6]							
D7	D6	D5	D4	D3	D2	D1	D0
MSB							LSB

INITIALIZE RANGE FIELD

If this field (flag) is set, the Signal Generator, upon receiving the next 1-PPS pulse, starts the I and Q coders.

DISABLE PRN CODE (I) FIELD

If this field (flag) is set, the Signal Generator does not use the I PRN codes in modulation.

DISABLE MESSAGE (I) FIELD

If this field (flag) is set, the Signal Generator does not use the I message symbols in modulation.

SELECT BPSK OR QPSK MODULATION MODE FIELD

If this field (flag) is set, the Signal Generator operates in the QPSK mode of modulation. If this field is not set, the Signal Generator operates in the BPSK mode of modulation.

DISABLE NH/MANCHESTER (Q) FIELD

If this field (flag) is set, the Signal Generator disables the NH code for dataless operation or Manchester Code for data operation.

DISABLE NH/MANCHESTER (I) FIELD

If this field (flag) is set, the Signal Generator disables the NH code for dataless operation or for the L5 I channel signal only, the Manchester Code for data operation. (Note that Manchester coding is not used on the L1 I channel signal).

DISABLE MESSAGE (Q) FIELD

If this field (flag) is set, the Signal Generator does not use the Q message symbols in modulation.

DISABLE PRN CODE (Q) FIELD

If this field (flag) is set, the Signal Generator does not use the Q PRN codes in modulation.

For clarity, the I and Q channel modulation formats which result from different combinations of control commands are tabulated below. Note that the I channel is always active so its data format does not depend on the D3 bit.

Table 15: Resulting I Modulation Format

D3	D1	D5	D2	PRN Code	Manchester Code	Neumann-Hoffman Code	Symbols
N/A	0	0	0	Enable	L5 Enable L1 Disable	Disable	Enable
N/A	0	0	1	Enable	Disable	Enable	Disable
N/A	0	1	0	Enable	Disable	Disable	Enable
N/A	0	1	1	Enable	Disable	Disable	Disable
N/A	1	0	0	Disable	L5 Enable L1 Disable	Disable	Enable

D3	D1	D5	D2	PRN Code	Manchester Code	Neumann-Hoffman Code	Symbols
N/A	1	0	1	Disable	Disable	Enable	Disable
N/A	1	1	0	Disable	Disable	Disable	Enable
N/A	1	1	1	Disable	Disable	Disable	Disable

Table 16: Resulting Q Modulation Format

D3	D7	D4	D6	PRN Code	Manchester Code	Neumann-Hoffman Code	Symbols
1	0	0	0	Enable	Enable	Disable	Enable
1	0	0	1	Enable	Disable	Enable	Disable
1	0	1	0	Enable	Disable	Disable	Enable
1	0	1	1	Enable	Disable	Disable	Disable
1	1	0	0	Disable	Enable	Disable	Enable
1	1	0	1	Disable	Disable	Enable	Disable
1	1	1	0	Disable	Disable	Disable	Enable
1	1	1	1	Disable	Disable	Disable	Disable
0	N/A	N/A	N/A	N/A	N/A	N/A	N/A

5.1.3.3 Initialization Command

This command specifies the initial range (modulo 1 second) value to be used by the Signal Generator. *Table 17* shows the initialization data fields for an L1 configured Signal Generator. *Table 18 on Page 31* shows the initialization data fields for an L5 configured Signal Generator at 500 SPS.

Table 17: L1 Initialization Command Fields

Byte Position	Description	Valid Range	Value / Scale Factor
Byte [7]	Symbol Rate/RF Configuration	0 or 128	Set to zero '0'
Byte [8]	Sub-Chip	0 – 255	Initial DDS Sub-Chip
Byte [9:10]	Code Chip Advance	0 – 1022	Initial Code Chip Advance
Byte [11:12]	Symbol Advance and Symbol 1 ms epoch	Bits [0:14] = 0 – 499 Bit [15:15] = 0-1 (MSB)	Initial Symbol Advance and Symbol 1 ms epoch
Byte [13:14]	I coder init G2. Byte[13] = init bits 0-7 Byte[14] = init bits 8-9		G2(I) channel coder initialization value at zero chip count

Byte Position	Description	Valid Range	Value / Scale Factor
Byte [15:16]	Q coder init G2. Byte[15] = init bits 0-7 Byte[16] = init bits 8-9		G2(Q) channel coder initialization value at zero chip Count. Set to zero if not used.

Table 18: L5 Initialization Command Fields 500 SPS

Byte Position	Description	Valid Range	Value / Scale Factor
Byte [7]	Symbol Rate/RF Configuration	0 or 128	Set to zero '0'
Byte [8]	Sub-Chip	0 – 255	Initial Sub-Chip Load
Byte [9:10]	Code Chip Advance	0 – 10229	Initial Code Chip Advance
Byte [11:12]	Symbol Advance and Symbol 1 ms epoch	Bits [0:14] = 0 – 499 Bit [15:15] = 0-1 (MSB)	Initial Symbol Advance and Symbol 1 ms epoch
Byte [13:14]	I coder init XB(I). Byte[13] = init bits 0-7 Byte[14] = init bits 8-12		XB(I) I channel coder initialization value at zero chip count.
Byte [15:16]	Q coder init XB(Q). Byte[15] = init bits 0-7 Byte[16] = init bits 8-12		XB(Q) Q channel coder initialization value at zero chip count.

SYMBOL RATE FIELD/RF CONFIGURATION FIELD

The message symbol rate sets the Symbols per Second (SPS) bit. When 0, the symbol rate is 500 SPS. When 1, the symbol rate is 1000 SPS (not currently supported—reserved for future use).

The RF Center frequency is set by the RF Center bit. When 0, the default RF frequency is chosen (1227.6 MHz for L1 and 1176.45 MHz for L5). When 1, the alternate frequency is chosen (1575.42 MHz for L1 and 1227.6 MHz for L5).

Table 19: Symbol Rate/RF Configuration Field

Byte [7]							
D7	D6	D5	D4	D3	D2	D1	D0
MSB							LSB
RF Center							SPS

SUB-CHIP FIELD

This value specifies the initial sub-chip phase to be loaded into the Code DDS in increments of 1/256 code chip. *Table 20* shows the Sub-Chip field byte and bit format.

Table 20: Sub-Chip Field

Byte [8]							
D7	D6	D5	D4	D3	D2	D1	D0
MSB							LSB

CODE CHIP ADVANCE FIELD

This value specifies the initial code chip advance from zero chip count. *Table 21* shows the Chip Advance field byte and bit format.

Table 21: Code Chip Advance Field

LS Byte [9]								MS Byte [10]							
D7	D6	D5	D4	D3	D2	D1	D0	D15	D14	D13	D12	D11	D10	D9	D8
							LSB	MSB							

SYMBOL ADVANCE FIELD

This value specifies the initial symbol epoch advance from zero epoch count. At 500 SPS, the symbol epoch is 2 ms, at 1000 SPS, the symbol epoch is 1 ms. *Table 22* shows the Symbol Advance field bit format. If 500 SPS is selected, the MSB indicates which 1 ms epoch is selected within the initial symbol epoch. A '0' indicates that the even 1 ms epoch is selected within the initial 2 ms symbol epoch. A '1' indicates that the odd 1 ms epoch is selected within the 2 ms symbol epoch.

Table 22: Symbol Advance Field

LS Byte [9]								MS Byte [10]							
D7	D6	D5	D4	D3	D2	D1	D0	D15	D14	D13	D12	D11	D10	D9	D8
							LSB	MSB							

L1 I CHANNEL G2 CODER INITIALIZATION FIELD

This field contains the initial state (10 bits) of the L1 I Channel G2 code generator. See *Table 23* for the I channel G2 coder initialization field bit format.

Table 23: L1 I Channel G2 Coder Initialization Field

LS Byte [13]								MS Byte [14]							
D7	D6	D5	D4	D3	D2	D1	D0	-	-	-	-	-	-	D9	D8
							LSB	MSB							
G2I(7)	(6)	(5)	(4)	(3)	(2)	(1)	G2I(0)	-	-	-	-	-	-	G2I(9)	G2I(8)

L1 Q CHANNEL G2 CODER INITIALIZATION FIELD

This field contains the initial state (10 bits) of the L1 Q Channel G2 code generator. If this field is set to zero, then the Q Channel G2 coder does not participate in modulation. See *Table 24 on Page 33* for the Q channel G2 coder initialization field bit format.

Table 24: L1 Q Channel G2 Coder Initialization Field

LS Byte [15]								MS Byte [16]						
D7	D6	D5	D4	D3	D2	D1	D0	-	-	-	-	-	D9	D8
							LSB	MSB						
G2Q(7)	(6)	(5)	(4)	(3)	(2)	(1)	G2Q(0)	-	-	-	-	-	G2Q(9)	G2Q(8)

L5 I CODER INIT XB(I) FIELD

This field contains the initial state (13 bits) of the L5 I Channel XB(I) code generator. See *Table 25* for the I channel XB(I) coder initialization field bit format.

Table 25: L5 I Channel XB(I) Coder Initialization Field

LS Byte [13]								MS Byte [14]							
D7	D6	D5	D4	D3	D2	D1	D0	-	-	-	D12	D11	D10	D9	D8
							LSB	MSB							
XBI(7)	(6)	(5)	(4)	(3)	(2)	(1)	XBI(0)	-	-	-	XBI(12)	11	10	9	XBI(8)

L5 Q CODER INIT XB(Q) FIELD

This field contains the initial state (13 bits) of the L5 Q Channel XB(Q) code generator. If this field is set to zero, the Q Channel XB(Q) coder does not participate in modulation. *Table 26* shows the byte and bit ordering for the Q channel XB(Q) coder initialization field.

Table 26: L5 Q Channel XB(Q) Coder Initialization Field

LS Byte [15]								MS Byte [16]							
D7	D6	D5	D4	D3	D2	D1	D0	-	-	-	D12	D11	D10	D9	D8
							LSB	MSB							
XBQ(7)	(6)	(5)	(4)	(3)	(2)	(1)	XBQ(0)	-	-	-	XBQ(12)	11	10	9	XBQ(8)

5.1.3.4 Code Chip Rate and Carrier Frequency Command

The Code Chip Rate and Carrier Frequency Command specifies in absolute terms, the new Code Chip Rate and Carrier Frequency (for either L1 or L5) to be assigned at the next 1PPS update pulse and the Code Chip Rate Ramp and Carrier Frequency Ramp to be assigned at the update periods following the next 1PPS update pulse. The Code Chip Rate Ramp Rate or Carrier Frequency Ramp can be set to zero if no ramp update is to be performed every update period (250 ms). If the Code Chip Rate Ramp Rate is not zero, then the Code Chip Rate is adjusted by the Code Chip Rate Ramp amount every 250 ms update period for three update periods following the next 1PPS. If the Carrier Frequency Ramp is not zero, then the Carrier Frequency is adjusted by the Carrier Frequency Ramp amount every 250 ms update period for three update periods following the next 1PPS. *Figure 10 on Page 35* shows the application of three ramp values (Δf_n) over 1 s application periods. The fourth one is overridden with the application of the next Carrier Frequency value (f_{n+1}). *Table 27 on Page 34* shows all fields applicable to this command.

Table 27: L1/L5 Code Chip Rate and Carrier Frequency Command Fields

Byte Position	Description	Valid Range	Scale Factor
Data Byte [17:22]	Code Chip Rate	1.023 ±0.25/1540 Mcps (L1) 10.23 ±0.25/115 Mcps (L5)	LSB = 75×2^{-48} Mcps
Data Byte [23:24]	Code Chip Rate Ramp	$\pm 8.525 \times 10^{-6}$ cps/250 ms (L1) $\pm 8.525 \times 10^{-5}$ cps/250 ms (L5)	LSB = 75×2^{-50} Mcps/250 ms
Data Byte [25:30]	Carrier Frequency	70 ±0.25 MHz	LSB = 300×2^{-48} MHz
Data Byte [31:33]	Carrier Frequency Ramp	±0.025 Hz/250 ms	LSB = 300×2^{-50} MHz/250 ms

CODE CHIP RATE FIELD

The Code Chip Rate field specifies the absolute initial code clock frequency. *Table 28* shows the byte and bit ordering for the Code Chip Rate field.

Table 28: Code Chip Rate Field

Byte [17]	Byte [18]	Byte [19]	Byte [20]	Byte [21]	Byte [22]
D7 – D0	D15 – D8	D23 – D16	D31 – D24	D39 – D32	D47 – D40
D0 = LSB					D47 = MSB

CODE CHIP RATE RAMP FIELD

This field is a 16 bit signed value (2's complement) where D15, the most significant bit is the sign bit. See *Table 29* for the Code Chip Rate Ramp field bit format.

Table 29: Code Chip Rate Ramp Field

LS Byte [23]								MS Byte [24]							
D7	D6	D5	D4	D3	D2	D1	D0	-	D14	D13	D12	D11	D10	D9	D8
							LSB	MSB(sign)							

CARRIER FREQUENCY FIELD

The Carrier Frequency Command specifies in absolute terms, the new Carrier Frequency (for either L1 or L5) to be assigned at the next 1PPS update pulse. See *Table 30* for the Carrier Frequency field byte and bit order format.

Table 30: Carrier Frequency Field Bit Format

Byte [25] LS Byte	Byte [26]	Byte [27]	Byte [28]	Byte [29]	Byte [30] MS Byte
D7 – D0	D15 – D8	D23 – D16	D31 – D24	D39 – D32	D47 – D40
D0 = LSB					D47 = MSB

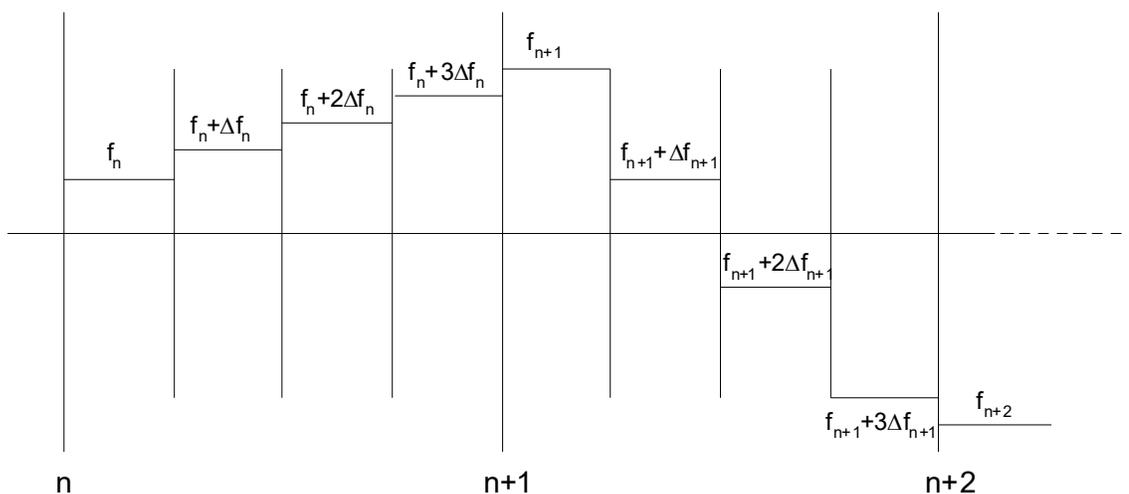
CARRIER FREQUENCY RAMP FIELD

This field is a 24 bit signed value (2's complement) where the most significant bit (D23) is the sign bit. See *Table 31* for the Carrier Frequency Ramp field byte and bit order format.

Table 31: Carrier Frequency Ramp Field Bit Format

Byte[31] – LS Byte								Byte[32]								Byte[33] – MS Byte							
D7 – D0								D15 – D8								D23 – D16							
7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	23	22	21	20	19	18	17	16
D0 = LSB																D23 = MSB							

Figure 10: Application of Frequency/Chipping Rate Ramp



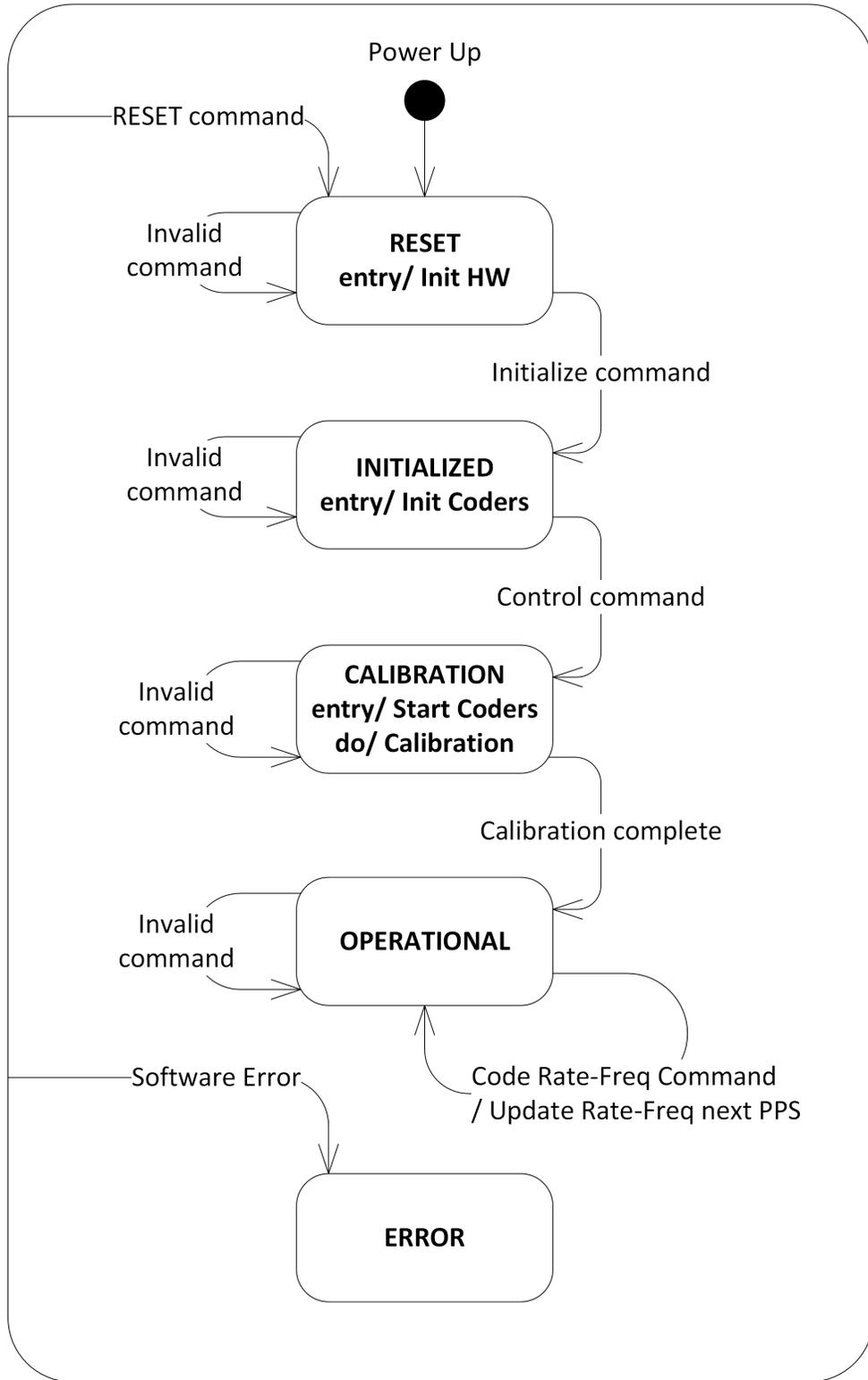
5.1.3.5 Reset Command

The Reset Command allows the Signal Generator to be put into a reset state when operational. When this command is received, the Signal Generator performs the actions as shown in *Figure 11 on Page 36*. There are no data fields associated with this command.

5.1.3.6 Watchdog Timer

The watchdog performs a Signal Generator board reset if it is not serviced for 3 seconds due to a software failure. The software services the watchdog as frequently as possible to prevent the watchdog from resetting the digital board under normal operating conditions.

Figure 11: Input Command Flowchart



5.1.4 Status Message

The Status Message contains the status message fields. The L1/L5 Signal Generator sends the Status Message to the WMP after every 1PPS update pulse. The status message contains the uplink range, the current setting of option switches, any errors that may have occurred in the last 1 second epoch and hardware status. The status message is transmitted from byte [0] through [33]. The WMP may need to swap bytes accordingly in order to recover the original data field (prior to transmission by the Signal Generator). The following sections indicate the data fields for a status message.

Table 32: Status Message Fields

Field	Bytes	Byte Position	Description
3-1	2	Byte [5:6]	Uplink Range Code Chip Sub-Phase
3-2	2	Byte [7:8]	Uplink Range Code Chip Counter
3-3	2	Byte [9:10]	Uplink Range Symbol Counter
3-4	1	Byte [11:11]	Switch Status
3-5	2	Byte [12:13]	Error Status
3-6	1	Byte [14:14]	Hardware Status
3-7	1	Byte [15:15]	For future use. Set to zero.
3-8	4	Byte [16:19]	Reset Command Second Epoch Counter Range = 0 – (2 ³¹ -1)
3-9	4	Byte [20:23]	Hardware Reset Second Epoch Counter Range = 0 – (2 ³¹ -1)
3-10	2	Byte [24:25]	Firmware Version Number
3-11	2	Byte [26:27]	FPGA Version Number
3-12	1	Byte [28:28]	Signal Generator State
3-13	5	Byte [29:33]	For future use. Set to zero.

Table 33: Uplink Range Fields

Data Byte Position	Description
Byte [5:6]	Uplink Range Code Chip Sub-Phase Resolution = 1 x 2 ⁻¹⁶ code chip
Byte [7:8]	Uplink Range Code Counter
Byte [9:10]	Uplink Range Symbol Counter

5.1.4.1 Uplink Range Code Chip Sub-Phase Field

This field contains the sub-phase of the code chip latched, within the current 1 ms epoch, upon detection of a 1PPS update pulse. *Table 34 on Page 38* shows the Uplink Range Code Chip Sub-Phase field byte and bit order.

Table 34: Uplink Range Code Chip Sub-Phase Field

LS Byte [5]								MS Byte [6]							
D7	D6	D5	D4	D3	D2	D1	D0	D15	D14	D13	D12	D11	D10	D9	D8
							LSB	MSB							

5.1.4.2 Uplink Range Code Chip Counter Field

This field contains the code count latched, within the current 1 ms epoch, upon detection of a 1PPS update pulse. *Table 35* shows the Uplink Range Code Counter field byte and bit order.

Table 35: Uplink Range Code Chip Counter Field

LS Byte [7]								MS Byte [8]							
D7	D6	D5	D4	D3	D2	D1	D0	D15	D14	D13	D12	D11	D10	D9	D8
							LSB	MSB							

5.1.4.3 Uplink Range Symbol Counter Field

This field contains the symbol count latched, within the current 1 ms epoch, upon detection of a 1PPS update pulse. At 500 SPS, the symbol counter epoch is 2 ms. At 1000 SPS, the symbol counter epoch is 1 ms. *Table 36* shows the Uplink Range Symbol Counter field byte and bit order. If 500 SPS is selected, the MSB indicates which 1 ms epoch is selected within the initial symbol epoch. A '0' indicates that the even 1 ms epoch is latched within the initial 2 ms symbol epoch. A '1' indicates that the odd 1 ms epoch is latched within the 2 ms symbol epoch.

Table 36: Uplink Range Symbol Counter Field

LS Byte [9]								MS Byte [10]							
D7	D6	D5	D4	D3	D2	D1	D0	D15	D14	D13	D12	D11	D10	D9	D8
							LSB	MSB							

5.1.4.4 Switch Status Fields

The Switch Status field contains the current state of all Signal Generator switches. The switch settings are polled when the Status Message is created at the start of the current 1 second epoch. *Table 37* shows the Switch Status field byte and bit order. *Table 38 on Page 38* shows the Switch Status bit fields.

Table 37: Switch Status Field

Byte [11]							
D7	D6	D5	D4	D3	D2	D1	D0
MSB							LSB

Table 38: Switch Status Bit Fields

Bit	Switch Status Description	Range
D0	TX Inhibit	0 = Enable 1 = Disable

Bit	Switch Status Description	Range
D1	IF Switch Position	0 = Enable 1 = Disable
D2	CW Mode only	0 = Not CW Mode 1 = CW Mode
D3-D7	Reserved for future use. Set to zero.	

TX INHIBIT FIELD

This flag indicates the TX Inhibit status of the Message interface. If a '1', this flag indicates if the transmitter has been disabled through the Message Interface. If a '0' this flag indicates that the Message interface has not disabled the transmitter.

IF SWITCH POSITION FIELD

This flag indicates the current setting of the IF switch. If a '1', this flag indicates that the IF switch has been disabled. If a '0', this flag indicates that the IF switch is enabled.

CW MODE ONLY FIELD

This flag indicates the current setting of the CW Only mode Switch. If a '1', this flag indicates that the CW Mode Only Switch is closed and that the Signal Generator is in CW mode only. If a '0', this flag indicates that the CW Mode Only Switch is open and that the Signal Generator is not in CW mode

5.1.4.5 Error Status Fields

The Error Status field contains any errors that may have occurred during the last 1 second epoch. The Error Status field bits are reset to zero after the status message is sent. *Table 39* shows the Error Status field byte and bit order. *Table 40 on Page 39* shows the Error Status bit fields.

Table 39: Error Status Field

LS Byte [12]								MS Byte [13]							
D7	D6	D5	D4	D3	D2	D1	D0	D15	D14	D13	D12	D11	D10	D9	D8
							LSB	MSB							

Table 40: Error Status Bit Fields

Bit	Error Status Description	Range
D0	CMP Data Error, see <i>Section 5.2, Error Handling on Page 44</i>	0 = No Error 1 = Error
D1	Update Data not complete at 1PPS	0 = Complete 1 = Incomplete
D2	Status Data not Complete at 1PPS	0 = Complete 1 = Incomplete
D3	Parity Error on Received Data	0 = No Parity Error 1 = Parity Error

Bit	Error Status Description	Range
D4	Framing Error on Received Data	0 = No Error 1 = Error
D5	Overrun Error on Received Data	0 = No Error 1 = Error
D6	Receive Data Sync Error	0 = Valid Sync Byte 1 = No Valid Sync Byte
D7	Receive Data CRC16 Error	0 = Valid CRC Field 1 = No Valid CRC Field
D8	Invalid Field Value in Last Command Received	0 = Valid Field Value 1 = Invalid Field Value
D9	Invalid Range Fields	0 = Valid Range Fields 1 = Invalid Range Fields
D10-D15	Reserved for future use. Set to zero.	

CMP DATA ERROR FIELD

See Section 5.2, *Error Handling on Page 44*.

UPDATE DATA NOT COMPLETE AT 1PPS FIELD

If a '1', this flag indicates that a command received during the previous 1 second epoch was incomplete.

STATUS DATA NOT COMPLETE AT 1PPS FIELD

If a '1', this flag indicates that a status message was not transmitted completely during the previous 1-second epoch. This flag is reset after the status message has been transmitted.

PARITY ERROR ON RECEIVED DATA FIELD

If a '1', this flag indicates that the UART detected a parity error in one or more command bytes during the previous 1-second epoch. This flag is reset after the status message has been transmitted.

FRAMING ERROR ON RECEIVED DATA FIELD

If a '1', this flag indicates that the UART detected a framing error in one or more command bytes during the previous 1-second epoch. This flag is reset after the status message has been transmitted.

OVERRUN ERROR ON RECEIVED DATA FIELD

If a '1', this flag indicates that the UART detected an overrun error in one or more command bytes during the previous 1-second epoch. This flag is reset after the status message has been transmitted.

RECEIVE DATA SYNC ERROR FIELD

If a '1', this flag indicates that the Signal Generator did not receive a valid sync byte in a command packet during the previous 1-second epoch. This flag is reset after the status message has been transmitted.

RECEIVE DATA CRC ERROR FIELD

If a '1', this flag indicates that the Signal Generator detected an invalid CRC field in a command packet during the previous 1-second epoch. This flag is reset after the status message has been transmitted.

INVALID FIELD VALUE FIELD

If a '1', this flag indicates that the Signal Generator detected an invalid field value in the last command received, during the previous 1-second epoch. This flag is reset after the status message has been transmitted.

INVALID RANGE FIELDS FIELD

If a '1', this flag indicates that the range fields contained in this status message are invalid and should not be used.

5.1.4.6 Hardware Status Fields

The Hardware Status field contains the current state of the Signal Generator hardware. The hardware is polled when the Status Message is created at the start of the current 1 second epoch. *Table 41* shows the Hardware Status field bit order. *Table 42* shows the Hardware Status bit fields.

Table 41: Hardware Status Field

Byte [14]							
D7	D6	D5	D4	D3	D2	D1	D0
MSB							LSB

Table 42: Hardware Status Bit Fields

Bit	Hardware Status Description	Range
D0	Reference 10 MHz Present	0 = Not Present 1 = Present
D1	Clock Circuit Fault	0 = No Fault 1 = Fault
D2	RF Circuit Fault	0 = No Fault 1 = Fault
D3	BPSK or QPSK Mode Selected	0 = BPSK 1 = QPSK
D4	Reserved for future use.	
D5	Symbols Per Second 500	0 = 500 SPS 1 = 1000 SPS
D6	Signal Generator Operational	0 = Not Operational 1 = Operational
D7	Reference 1PPS present	0 = Not Present 1 = Present

10 MHZ PRESENT FIELD

This flag indicates if the 10 MHz clock signal is present. If a '1', then the 10 MHz signal is present. If a '0', then the 10 MHz signal is absent.

CLOCK CIRCUIT FAULT FIELD

This flag indicates if the clock circuit board is faulty. If a '1', then the clock circuit board is faulty. If a '0', then the clock circuit board is not faulty.

RF CIRCUIT FAULT FIELD

This flag indicates if the RF circuit board is faulty. If a '1', then the RF circuit board is faulty. If a '0', then the RF circuit board is not faulty.

BPSK OR QPSK MODE SELECTED

This flag indicates the modulation mode selected, BPSK or QPSK. If set to '0', then BPSK modulation mode is selected. If set to '1', then QPSK mode is selected. The value of this flag is determined by the BPSK/QPSK Modulation Mode Select bit, see *Table 13, L1/L5 Control Command Bit Fields on Page 28*.

SYMBOLS PER SECOND FIELD

This flag indicates the hardware symbol rate. If a '0', then the Signal Generator is processing 500 symbols per second. The Symbol Rate field in the L5 Initialization Command determines the value of this flag, see *Table 18, L5 Initialization Command Fields 500 SPS on Page 31*.

SIGNAL GENERATOR OPERATIONAL

This flag indicates if the Signal Generator is operational and that Code Rate Commands and Carrier Frequency Commands are accepted. If this bit is set to '0', Code Rate Commands and Carrier Frequency Commands are not applied. If this bit is set to '1', the Signal Generator is operational and Code Rate Commands and Carrier Frequency Commands are applied. This bit is only set to '0' at power-up and after a Reset Command is received. It is set to '1' after a Control Command is received and all internal calibrations have been performed.

REFERENCE 1PPS PRESENT FIELD

The flag indicates if the 1PPS reference is present. If this bit is set to '1', the 1PPS signal is present. If this bit is set to '0', the 1PPS signal is not present.

5.1.4.7 Reset Command Second Epoch Counter

This field contains the number of one second epochs counted since the last hardware reset occurred or since the last RESET command was received. The counter is started upon successful detection of an external 1PPS update pulse. The range of this field is $0 - (2^{31}-1)$. The MSB is set to zero to prevent false detection of packet SYNC header bytes. *Table 43* shows the byte order and format for this field.

Table 43: Reset Command Second Epoch Counter

LS Byte [16] D0 = LSB								Byte [17]								Byte [18]								LS Byte [19] D31 = MSB = '0'							
D7 – D0								D15 – D8								D23 – D16								D31 – D24							
7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	23	22	21	20	19	18	17	16	31	30	29	28	27	26	25	24

5.1.4.8 Hardware Reset Second Epoch Counter

This field contains the number of one second epochs counted since the last hardware reset occurred. The counter is started upon successful detection of an external 1PPS update pulse. The range of this field is $0 - (2^{31}-1)$. The MSB is set to zero to prevent false detection of packet SYNC header bytes. *Table 44 on Page 42* shows the byte order and format for this field.

Table 44: Hardware Reset Second Epoch Counter

LS Byte [20] D0 = LSB								Byte [21]								Byte [22]								LS Byte [23] D31 = MSB = '0'							
D7 – D0								D15 – D8								D23 – D16								D31 – D24							
7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	23	22	21	20	19	18	17	16	31	30	29	28	27	26	25	24

5.1.4.9 Firmware Version Number

This field contains the firmware version number. The firmware version number consists of two parts, the revision number (major) and the release (minor). *Table 45 on Page 43* shows the byte order and format for this field.

Table 45: Firmware Version Number Field

LS Byte [24]								MS Byte [25]							
D7	D6	D5	D4	D3	D2	D1	D0	D15	D14	D13	D12	D11	D10	D9	D8
							LSB	MSB							

5.1.4.10 FPGA Version Number

This field contains the FPGA version number. The FPGA version number consists of two parts, the revision number (major) and the release (minor). *Table 46* shows the byte order and format for this field.

Table 46: FPGA Version Number Field

LS Byte [26]								MS Byte [27]							
D7	D6	D5	D4	D3	D2	D1	D0	D15	D14	D13	D12	D11	D10	D9	D8
							LSB	MSB							

5.1.4.11 Signal Generator State

This field contains the state of the Signal Generator during the previous one second epoch. *Table 47* shows the byte order and format for this field. *Table 48 on Page 43* shows the Signal Generator state values.

Table 47: Signal Generator State Field

Byte [28]							
D7	D6	D5	D4	D3	D2	D1	D0
MSB							LSB

Table 48: Signal Generator State Value

State Value	Description
0	Invalid State Error. This indicates a software error.
1	RESET state
2	INITIALIZED state
3	CALIBRATION state
4	OPERATIONAL state

5.1.5 CRC-16/CCITT Checksum Field

A CRC-16/CCITT Cyclic Redundancy Check field is used to validate the received message to a high degree of confidence that it was not corrupted during transmission. The sending system calculates the CRC-16 on all message bytes excluding the CRC data bytes, and appends it to the message. The receiving system calculates the CRC-16 on all message bytes received, excluding the CRC data bytes. The calculated CRC is compared with the received CRC. If the calculated CRC does not match the received CRC, the received message is declared as corrupted. A corrupted message is not used. *Table 49* shows the CRC-16/CCITT field and *Table 50 on Page 44* shows its bit format. The characteristics for the CRC-16/CCITT are shown in *Table 51 on Page 44*.

Table 49: CRC-16/CCITT Checksum Field

Field	Bytes	Byte Position	Description	Range
4	2	Byte [34:35]	CRC16 Checksum	Hex 0000 – FFFF

Table 50: CRC-16/CCITT Checksum Field

LS Byte [34]								MS Byte [35]							
D7	D6	D5	D4	D3	D2	D1	D0	D15	D14	D13	D12	D11	D10	D9	D8
							LSB	MSB							

Table 51: CRC-16-CCITT Characteristics

Name	CRC-16/CCITT
CRC Width	16 Bits
Polynomial	$1021 = X^{16} + X^{12} + X^5 + X^0$
Initial CRC Value	0xFFFF Hex
Input Bytes Reflected?	NO
Output CRC Result Reflected?	NO
Output XOR Value	0x0000
Single Bit Errors Detected	100%
Double Bit Errors Detected	100%
Odd Numbered Bit Errors Detected	100%
Burst Errors Shorter Than 16 Bits	100%
Burst Errors of Exactly 17 Bits	99.9968%
All Other Burst Errors	99.9984%

5.2 Error Handling

Table 52 shows the Signal Generator error conditions and their corresponding handling methods.

Table 52: Errors

Error Description	Handling Method	Notes
CMP message truncated	I and Q set to zero and Transmitter disabled	Report status
CMP MSGRDY stuck high	I and Q set to zero and Transmitter disabled	Report status
CMP MSGRDY stuck low	I and Q set to zero and Transmitter disabled	Report status
MSGDATA not ready when needed	I and Q set to zero and Transmitter disabled	Report status

As described in *Chapter 1*, the Signal Generator is comprised of two independent L1 and L5 generators. Each digital card has the same firmware (program software). The firmware is stored in on-board, non-volatile memory, which allows the Signal Generator's firmware to be updated in the field. Thus, updating firmware takes only a few minutes instead of the several days which would be required if the Signal Generator had to be sent to a service depot.

When updating to a higher revision level, you will need to transfer the new firmware to the appropriate card using WinLoad, a Windows-based program. It is recommended that you use the most recent version of WinLoad available.

Below is shown an outline of the procedure for updating your Signal Generator's firmware:

1. Contact the NovAtel Customer Support (refer to Contact Information on Page 8 for contact options)
2. Download update files
3. Decompress files
4. Run the firmware loading utility

6.1 Contacting the NovAtel Customer Support

The first step in updating the Signal Generator is to contact the NovAtel Customer Support using the contact information on *Page 8*.

When you call, be sure to have the WAAS GUS Signal Generator's serial number and program revision level available. This information is printed on the rear panel of the Signal Generator, as shown in Figure 12.

Figure 12: Serial Number and Version Label



You can also verify the information. First power up the Signal Generator and then communicate with it using your custom interface to check the Signal Generator's version. See also *Section 5.1.4.9, Firmware Version Number* on *Page 43*.

After conferring with the NovAtel Customer Support to establish the required revision level, as well as the terms and conditions of your firmware update, the NovAtel Customer Support will issue you with the latest firmware when it is available.

If it is determined that you will be updating to a higher revision level with the use of the firmware loading utility, the NovAtel Customer Support will confirm with you as to the procedures, files, and methods required for using this utility. As the main utility and other necessary files are generally provided in a compressed file format, you will also be given a file decompression password. The utility and update files are available from NovAtel Customer Support.

6.2 Downloading the Files

Typically, there are three files required when performing firmware updates on a particular Signal Generator card:

- WINLOAD.EXE (the firmware loading utility program)
- [Application Firmware File Name].HEX (the Application firmware update file)
- [FPGA Firmware File Name].HEX (the FPGA firmware update file)

For example, the Signal Generator Application and FPGA firmware files might be named SIGGEN-2.10.HEX and SIGGEN-FPGA-2.9.HEX respectively.

To proceed with your update, you will first need to download the appropriate files. Contact NovAtel Customer Support: support@novatel.com.

The files are available in compressed, password-protected file format. The compressed form of the files may have different names than the names discussed above; NovAtel Customer Support will advise you as to the exact names of the files you need. As well, NovAtel Customer Support will provide you with a file de-compression password.

6.3 Decompressing the Files

After copying the compressed files to an appropriate directory on your computer, each file must be decompressed.

A Windows-based dialog is provided for password entry.

The self-extracting archive then generates the following files:

WinLoad.exe	WinLoad utility program
HowTo.txt	Instructions on how to use the WinLoad utility
WhatsNew.txt	Information on the changes made in the firmware since the last revision
[Application Firmware File Name].hex	Application firmware version update file
[FPGA Firmware File Name].hex	FPGA firmware version update file

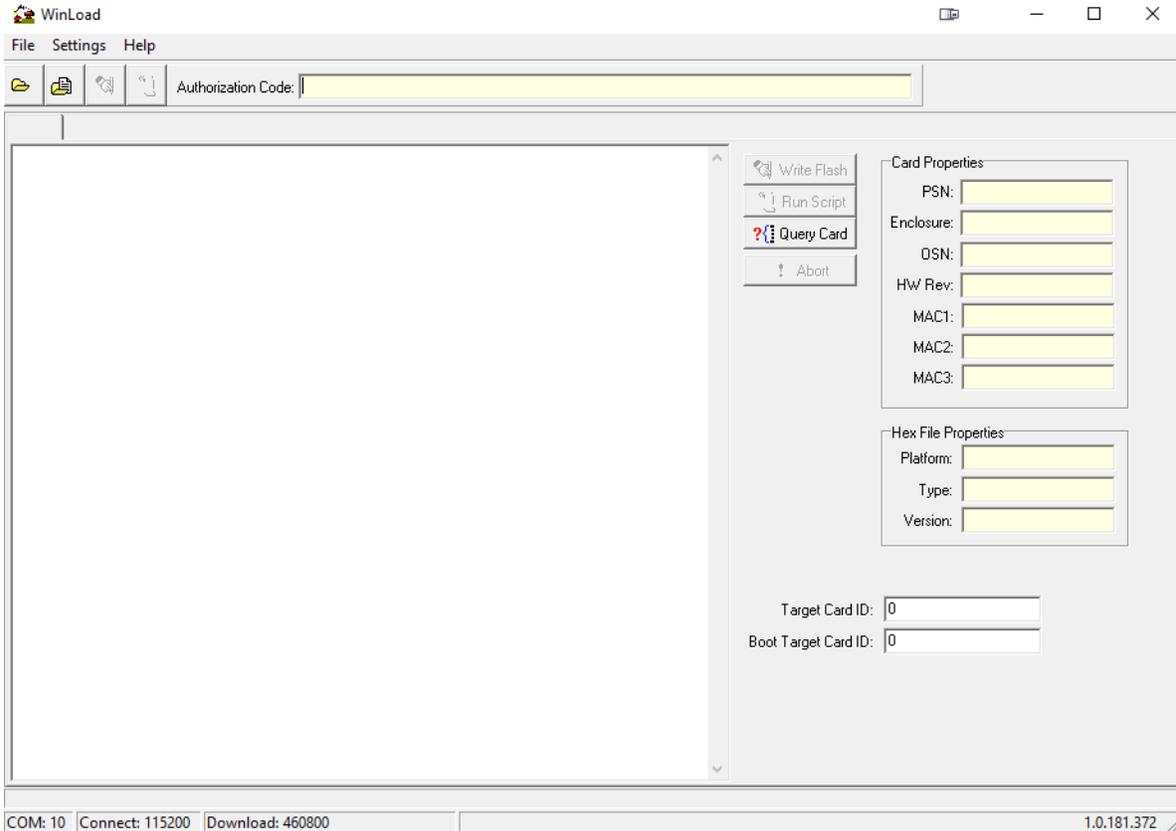
6.4 Running WinLoad

WinLoad is a Windows based program used to download firmware to Signal Generator cards. The main screen is shown in *Figure 13*. Note that in order to load firmware on to the WAAS GUS Signal Generator, the following hardware setup is required:

- Data Source Modules need to be connected to the L1 and L5 CMP ports and Code 1PPS Out ports. These also have to be connected to the PC which will perform the firmware load, or at a minimum need to be powered.
- The L1 and L5 WMP ports need to be connected to the PC which will perform the firmware load.
- A 1PPS signal needs to be provided into the 1PPS In port of the WAAS GUS Signal Generator.

Once these are in place, WinLoad can then be used to load firmware as described in the following sections.

Figure 13: Main Screen of WinLoad

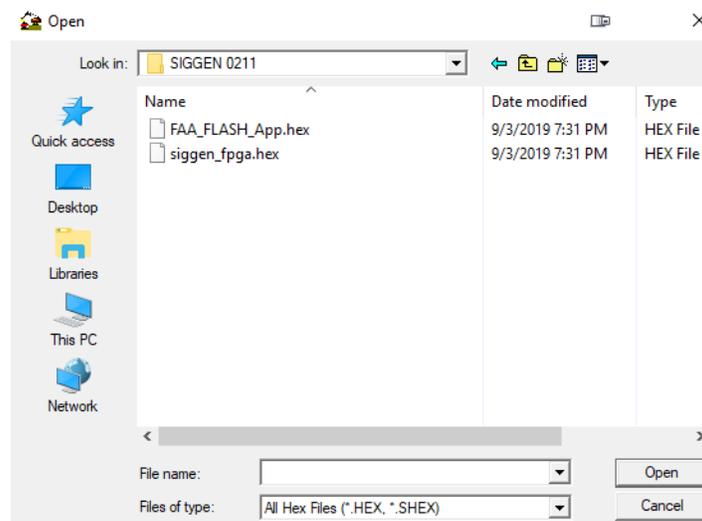


If you are running WinLoad for the first time you will need to make sure the file and communications settings are correct.

6.4.1 Open a File to Download

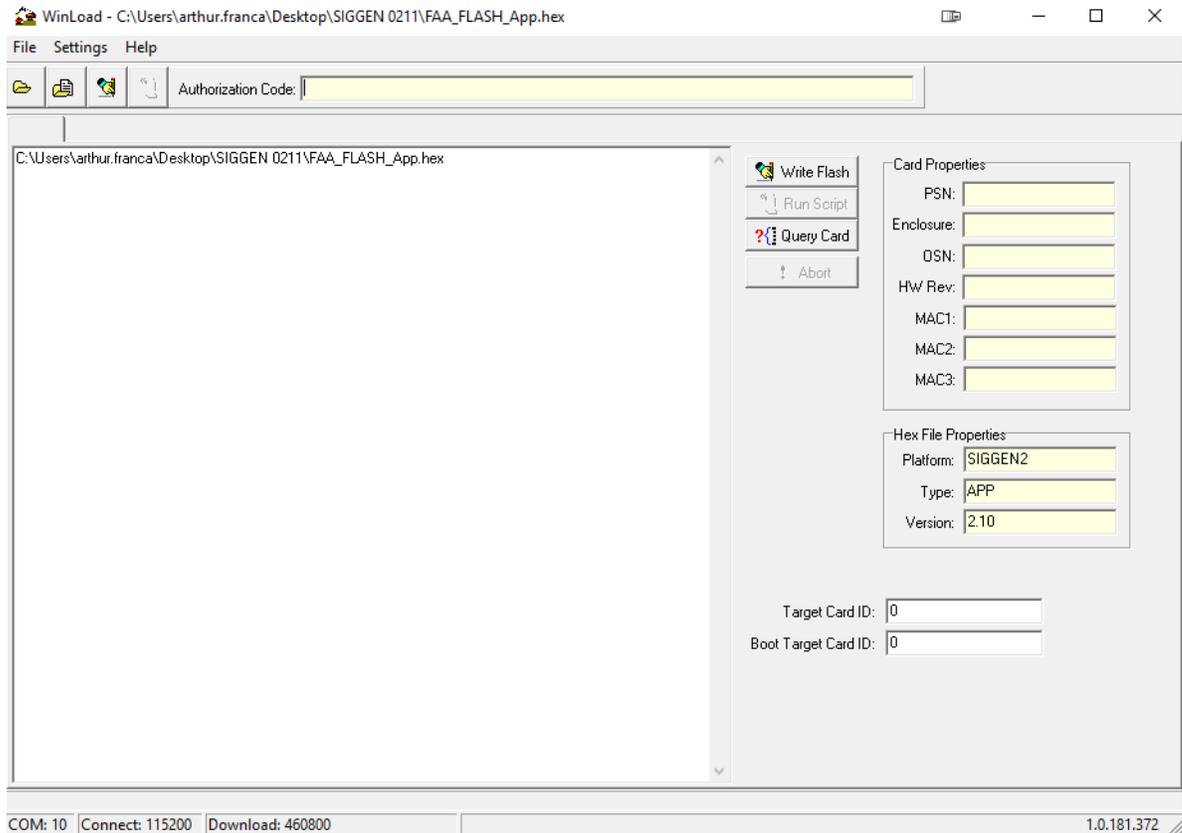
From the file menu choose Open. Use the Open dialog to browse for your file, see *Figure 14*.

Figure 14: WinLoad's Open Dialog



Once you have selected your file, the name should appear in the main display area and in the title bar, see *Figure 15*.

Figure 15: Open File in WinLoad



The *Target Card ID* field allows you to specify which Signal Generator card to update, see *Table 53* below.

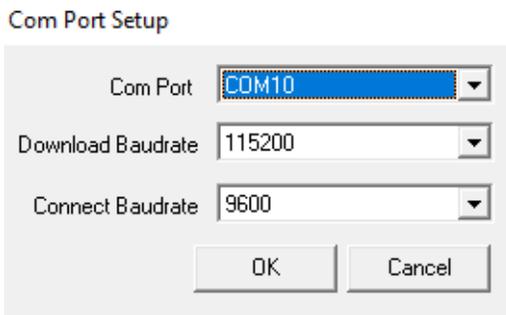
Table 53: Target Card Identification

Entry	Description
0	SigGen Digital Card

6.4.1.1 Communications Settings

To set the communications port and baud rate, select COM Settings from the Settings menu, see *Figure 16*. Choose the port on your PC from the Com Port drop down list and the baud rate from the Download Baudrate drop down list. The Download Baudrate can be set to 9600 or 115200 while the Connect Baudrate should be set to 9600.

Figure 16: COM Port Setup



6.4.2 Downloading firmware

To download firmware follow these steps:

1. Set up the communications port as described in *Communications Settings* above.
2. Select the file to download, see *Open a File to Download* on Page 48.
3. Make sure the file path and file name are displayed in the main display area, see *Figure 15* above.
4. Click on the *Write Flash* button to download the firmware:



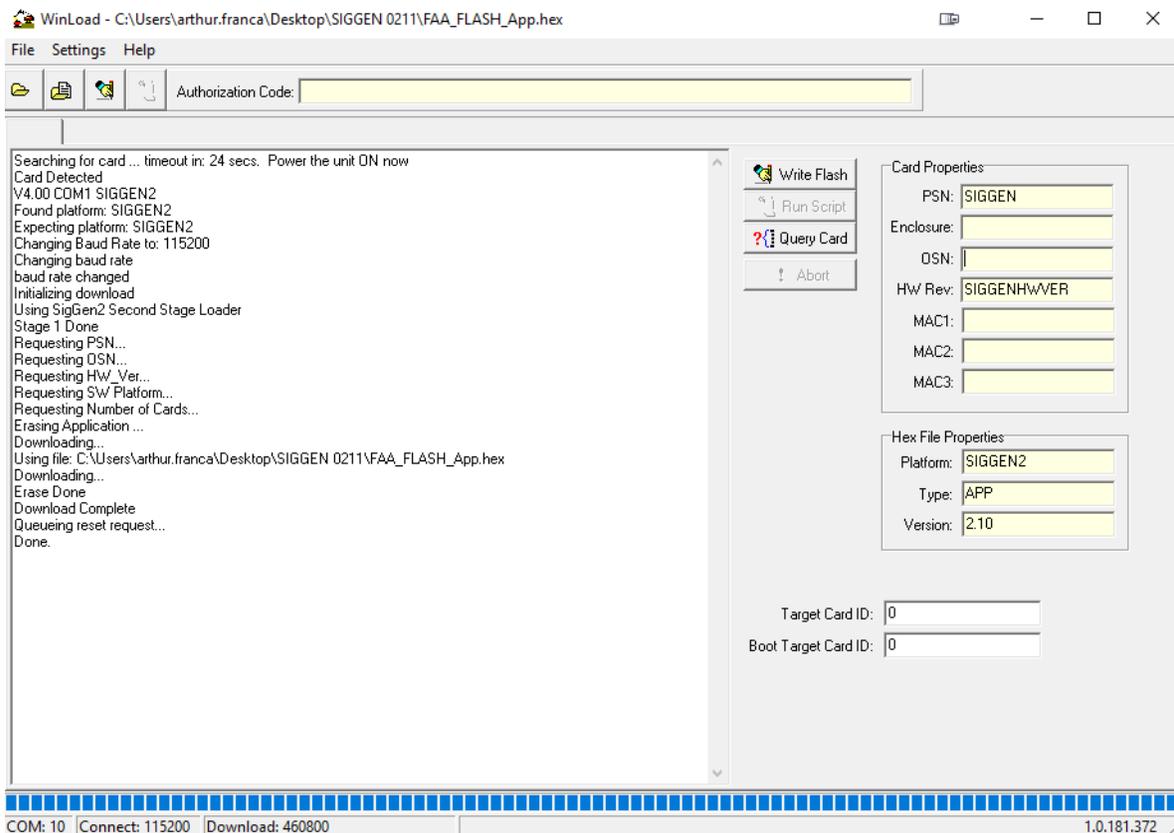
5. While WinLoad searches for the card, power cycle the Signal Generator (turn it off and then on again).



You will only be able to access information from the card and download new firmware during the first few seconds after power initiation.

6. WinLoad should be able to locate the card and the hex file should start downloading.
7. The Signal Generator should finish downloading and reset. The process is complete when “Done.” is displayed in the main display area, see *Figure 17*.

Figure 17: Update Process Complete



8. Close WinLoad.

This completes the procedure required to update a Signal Generator.

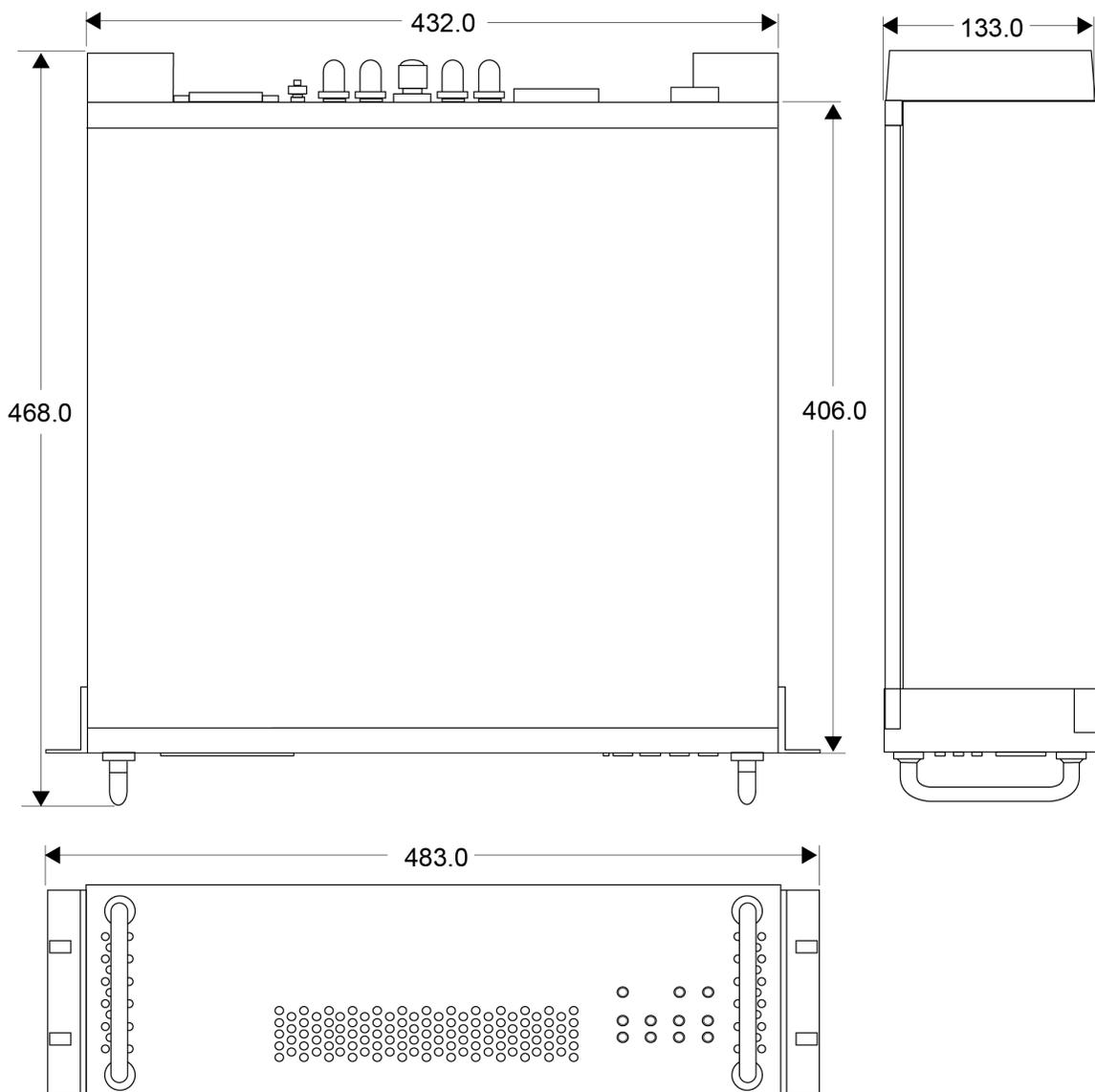


The L1 and L5 firmware loads are independent of each other and Application and FPGA firmware must be loaded individually for each.

A.1 Signal Generator

<i>PHYSICAL</i>	
Size	432 mm (17.0") x 406 mm (16.0") x 133 mm (5.2")
Weight	9.8 kilograms (21.4 lb.)
<i>MECHANICAL DRAWINGS</i>	

Figure 18: Signal Generator Dimensions



Dimensions are in millimeters.

ENVIRONMENTAL				
Operating Temperature	0° C to +50° C			
Storage Temperature	-40°C to +85°C			
Operating Humidity	10 to 80% non-condensing			
Storage Humidity	0 to 95% non-condensing			
INPUT/OUTPUT CONNECTORS				
Power Input	Input power connector - IEC 320-C14			
	3-pin power cord provided (for North American standard A/C)			
	Voltage	100 to 240 VAC* * Nominal power input voltage range to which an additional 10% tolerance is assumed.		
	Frequency	47 to 63 Hz		
	Current	0.3 A @ 120 VAC 0.2 A @ 230 VAC		
	VA	<75		
	Fuse Rating:	Glass 5x20 mm 2.5 A 250 VAC slow blow (there are 2 of these)		
Ground Screw	Length of Stud	3/8"		
	Stud Thread	8-32		
L1 WMP	DE9P Connector			
L5 WMP	DE9P Connector			
PPS Input	Connector	TNC female jack		
	Signal Description	A one-pulse-per-second normally high, active low pulse (between 10 microsecond to 1 millisecond) where the falling edge is the reference.		
	Level	Voltage	High > 2.0 VDC	
Low < 0.80VDC				
L1 or L5 1PPS Output	Connector	TNC female jack		
	Signal Description	A one-pulse-per-second normally high, active low 1 millisecond pulse where the falling edge is the reference		
	Level	Voltage	High >2.0 VDC Low < 0.4 VDC	
			Impedance	Open drain with 1k pullup Resistor to +5 V
L1 IF Output	Connector	TNC female jack		
	Frequency	70.000 MHz		
	Bandwidth	22 MHz		
	Level	-20 dBm ±1 dB		
	Impedance	50 Ω		
	VSWR	2:1 max at the center frequency		

L5 IF Output	Connector	TNC female jack	
	Frequency	70.000 MHz	
	Bandwidth	22 MHz	
	Level	-20 dBm \pm 1 dB	
	Impedance	50 Ω	
	VSWR	2:1 max at the center frequency	
L1 RF Output	Connector	Type N female jack	
	Frequency	Default: 1227.6 MHz (L2) Alternate: 1575.42 MHz (L1)	
	Bandwidth	22 MHz	
	Level	-50 dBm \pm 3 dB	
	Impedance	50 Ω	
	VSWR	2:1 max at the center frequency	
L5 RF Output	Connector	Type N female jack	
	Frequency	Default: 1176.45 MHz (L5) Alternate: 1227.6 MHz (L2)	
	Bandwidth	22 MHz	
	Level	-50 dBm \pm 3 dB	
	Impedance	50 Ω	
	VSWR	2:1 max at the center frequency	
10 MHz Input	Connector	TNC female jack	
	Sensitivity	13 \pm 1 dBm	
	Impedance	50 Ω	
10 MHz Output	Connector	TNC female jack	
	RF Output Power	3 \pm 3 dBm	
	Impedance	50 Ω	
	Phase Noise (internal OCXO only)	@10 Hz @100 Hz @1 kHz @10 kHz	-125 dBc/Hz max -155 dBc/Hz max. -165 dBc/Hz max. -165 dBc/Hz max.
	Temperature Stability (internal OCXO only)	\pm 1 \times 10 ⁻⁸ over operating temperature range	
	Aging (internal OCXO only)	5 \times 10 ⁻¹⁰ per day after 30 days operating (typical)	

A.1.1 Connector Pin-Outs

Table 54 and Table 55 show details of the connector pin-outs on the Signal Generator.

Table 54: L1 and L5 WMP Connector Pin-Out Descriptions

Pin No.	Direction	Name
1	Reserved	
2	Out	TxD
3	In	RxD
4	Reserved	
5	GND	
6	Reserved	
7	In	CTS
8	Out	RTS
9	Reserved	

Table 55: L1 and L5 CMP Connector Pin-Out Descriptions

Pin No.	Direction	Name
1	GND	
2	Out	MSGCLKa
3	In	MSGRDYa
4	Reserved	
5	In	MSGRDATaA
6	In	RESETa
7	GND	
8	Reserved	
9	In	TXINHb
10	Reserved	
11		
12		
13	In	MSGDATAb
14	Out	MSGCLKb
15	Reserved	
16	In	MSGRDYb
17	In	TXINHa
18	Reserved	
19		
20		
21		
22	In	RESETb
23	Reserved	
24		
25		

A.1.2 Cables

A.1.2.1 Power Cable

The power cable supplied with the Signal Generator connects from the Power Input port on the back of the Signal Generator to an external power source (+100 to +240 VAC). An input voltage outside of this range may physically damage the unit, voiding the warranty. The power supply automatically adapts its input power to the national power source in the country of use as long as it is within the above range and you have an adapter for your local power receptacle.

Figure 19: Power Cable



